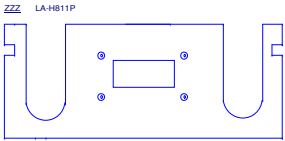


MODEL NAME : *Modena*
PCB NO : *LA-H811P*
BOM P/N : *451AHT31L01 ~ L32*



Dell/Compal Confidential

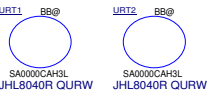
Schematic Document

(MODENA ICE Lake U)

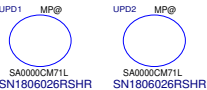
CPU Option



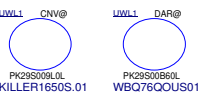
TBT Option



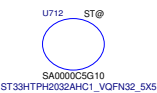
PD Option



WLAN Option



TPM Option



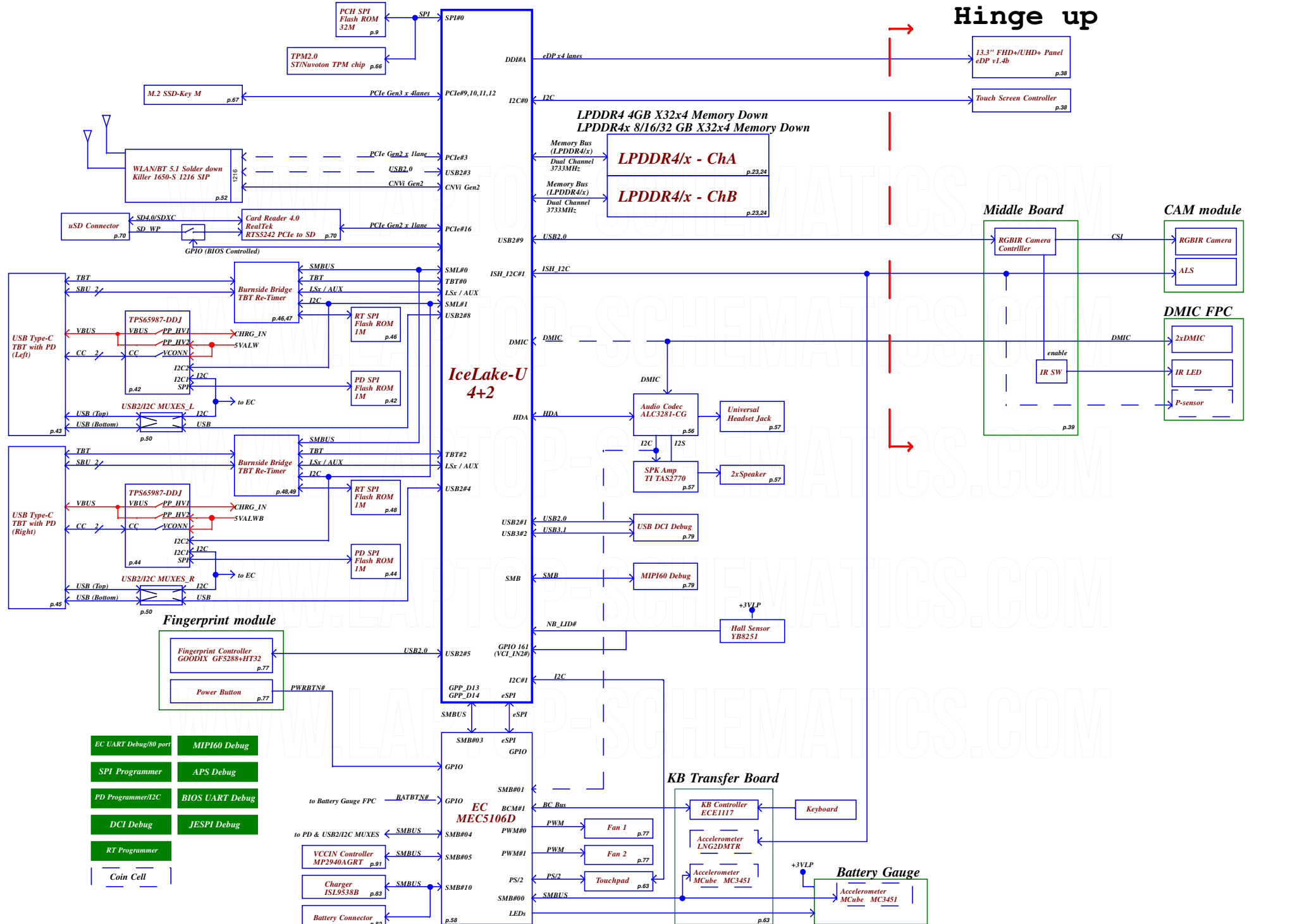
EC Option



2019-12-16

Rev: 1.0 (A00)

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				Size Document Number
				LA-H811P
				Rev 0.1 (000)
				Date: Tuesday, December 24, 2019 Sheet 1 of 100



Hinge Down

Hinge up

- EC UART Debug/80 port
- SPI Programmer
- PD Programmer/I2C
- DCI Debug
- RT Programmer
- MIP160 Debug
- APS Debug
- BIOS UART Debug
- JESPI Debug
- Coin Cell

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	PCB Revision
0	240K +/- 1%	4700p	X00	0.1
1	130K +/- 5%	4700p	X01	0.2
2	62K +/- 5%	4700p	X02	0.3
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	1K +/- 5%	4700p	N/A	N/A

SMBUS Control Table

	SOURCE	PCH	BATT Connector	Charger	VCCIN Controller	PD Controller	MIPI60	USB/I2C MUX	BurnSide Bridge	Accel	TI Amp.
PCH_SML0CLK PCH_SML0DATA	PCH								Reserve		
PCH_SML1CLK PCH_SML1DATA	PCH					V			V		
SMBCLK SMBDATA	PCH						V				
EC_SMB03_CLK EC_SMB03_DAT	MECS106	V									
EC_SMB04_CLK EC_SMB04_DAT	MECS106					V		V			
EC_SMB05_CLK EC_SMB05_DAT	MECS106				Reserve						
EC_SMB10_CLK EC_SMB10_DAT	MECS106		V	V							
EC_SMB00_CLK EC_SMB00_DAT	MECS106									V	
EC_SMB01_CLK EC_SMB01_DAT	MECS106										V

Check

PCIe/USB3.1

Flexible I/O	Interface	DESTINATION
0	PCI-E#1 / USB 3.1#1	None
1	PCI-E#2 / USB 3.1#2	USB DCI Debug
2	PCI-E#3 / USB 3.1#3	WLAN PCIe Gen2
3	PCI-E#4 / USB 3.1#4	None
4	PCI-E#5 / USB 3.1#5	None
5	PCI-E#6 / USB 3.1#6	None
6	PCI-E#7	None
7	PCI-E#8	None
8	PCI-E#9	M.2 SSD
9	PCI-E#10	
10	PCI-E#11 / SATA#0	
11	PCI-E#12 / SATA#1a	
12	PCI-E#13	None
13	PCI-E#14	None
14	PCI-E#15 / SATA#1b	None
15	PCI-E#16 / SATA#2	Card Reader PCIe GEN2

USB 2.0

USB 2.0 PORT#	DESTINATION
1	USB DCI Debug
2	None
3	None
4	Type-C_R
5	FPR
6	None
7	None
8	Type-C_L
9	CAM
10	BT

CLK

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	WLAN
	CLKOUT_PCIE1	M.2 SSD
	CLKOUT_PCIE2	None
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	None
	FLEX CLOCKS	DESTINATION
	ESPI_CLK	EC eSPI

Thunderbolt

	TBT PORT#	DESTINATION
TBT	0	USB Type-C_L
	1	None
	2	USB Type-C_R
	3	None

Displayport

	DDI PORT#	DESTINATION
DDI	A	4 Lane eDP
	B	None

Symbol Note :

@ : means de-pop

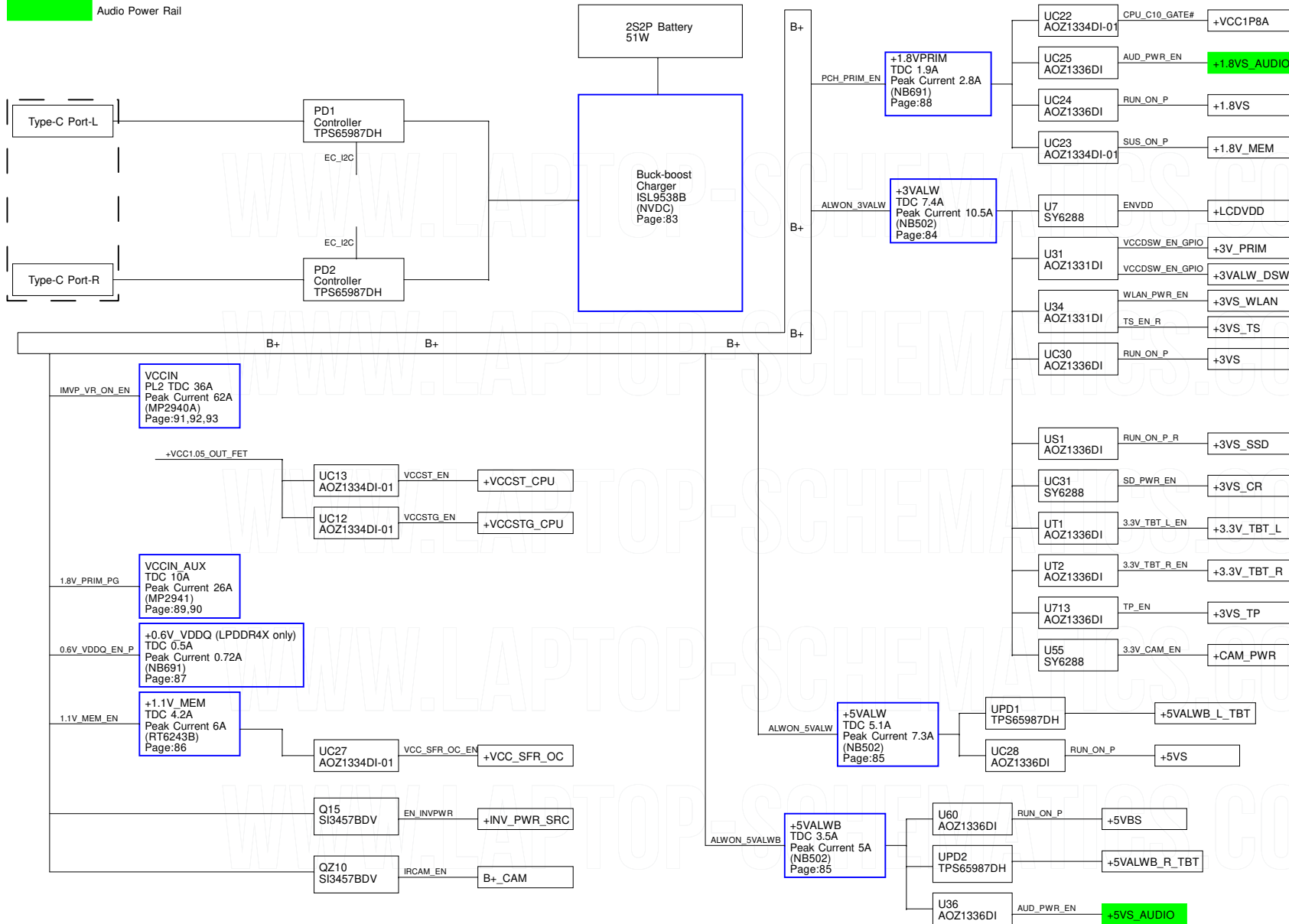
 : means Digital Ground

 : means Analog Ground

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Size	Document Number	Date	Yvesday, December 24, 2019	Rev 0.1 (X00)
	LA-H811P	Sheet	3	of 100

Modena POWER BLOCK DIAGRAM

Power Rail
Audio Power Rail

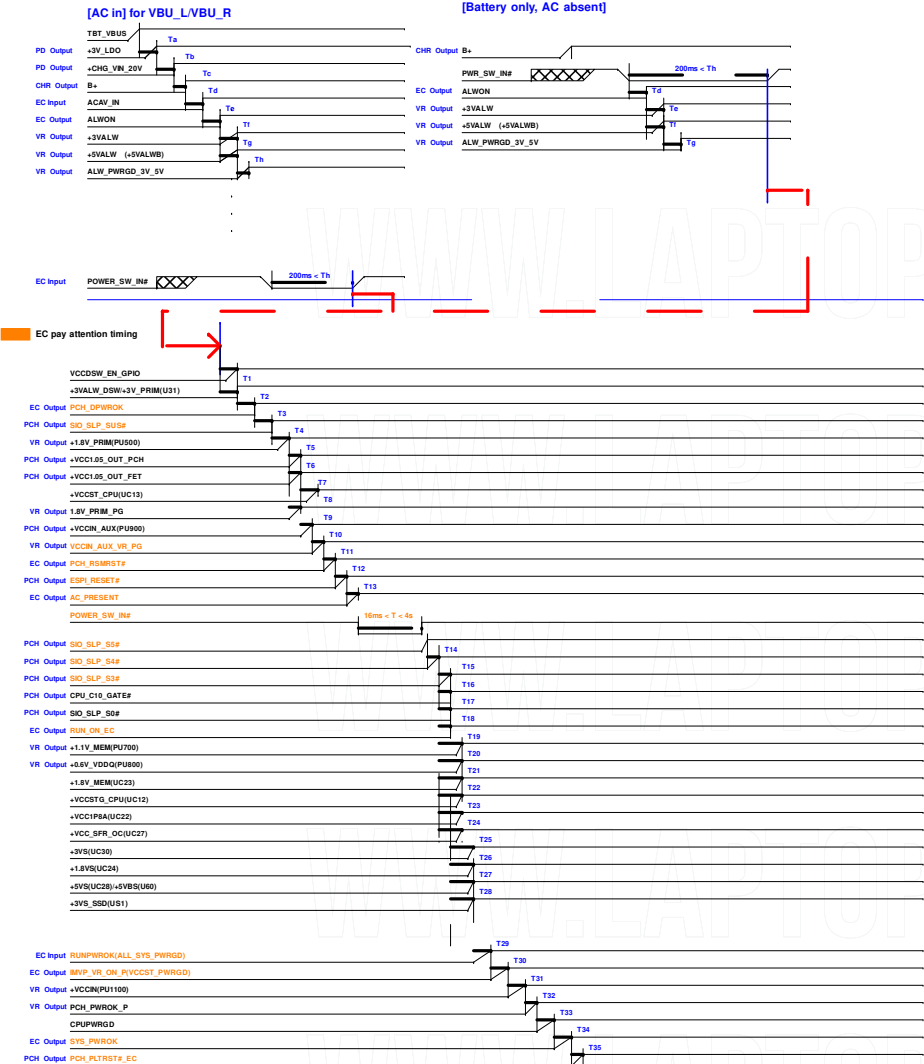


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Size	LA-H811P	Rev	0.1 (2025)	Page	1 of 1

Power On Sequence

[AC in]

[Battery only, AC absent]

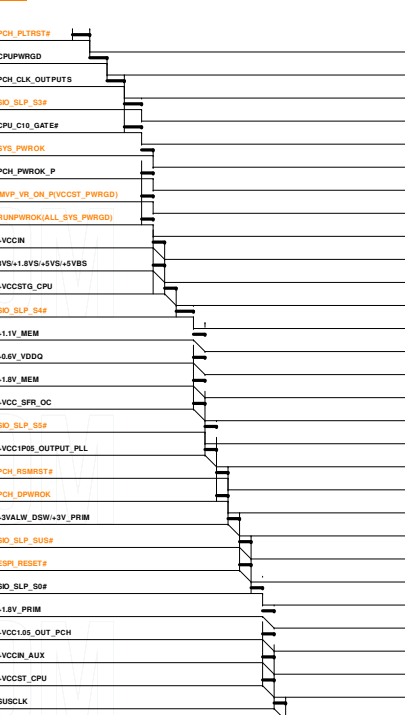


ITEM	Measure Point	Time
Ta	TBT_VBUS	To -3V_LDO
Tb	+3V_LDO	To -CHG_VIN_20V
Tc	+CHG_VIN_20V	To B+
Td	B+	To ACAA_IN
Te	ACAA_IN	To ALWON
Tf	ALWON	To -3VALW
Tg	ALWON	To -3VALW (+5VALWB)
Th	-3VALW	To ALW_PWRGD_3V_5V

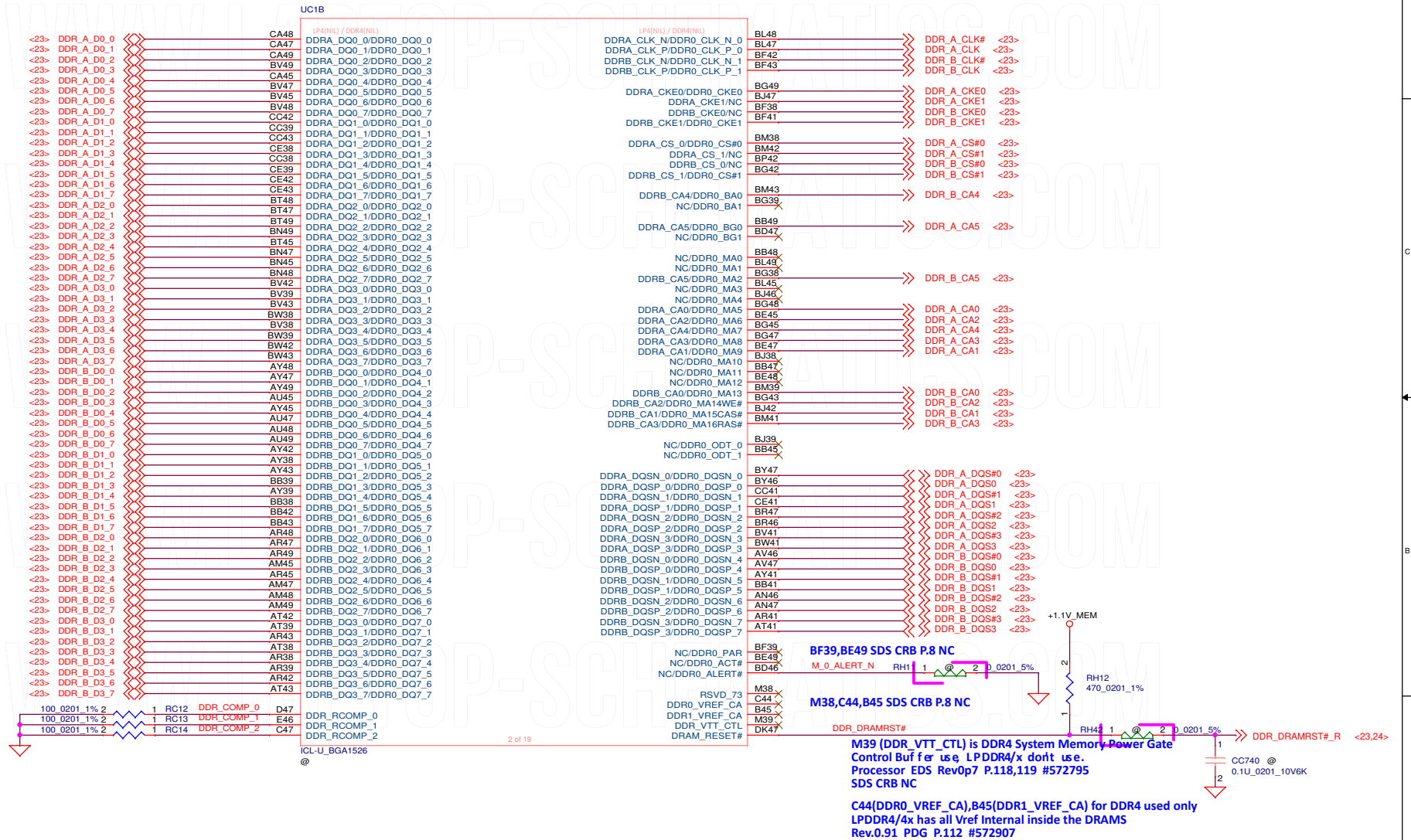
ITEM	Measure Point	Time
T1	VCCDSW_EN_GPIO	To -3VALW_DSW+3V_PRIM
T2	-3VALW_DSW+3V_PRIM	To PCH_DPWRK
T3	PCH_DPWRK	To SIO_SLP_SUS#
T4	SIO_SLP_SUS#	To +1.8V_PRIM
T5	+1.8V_PRIM	To +VCC1.05_OUT_PCH
T6	+1.8V_PRIM	To +VCC1.05_OUT_FET
T7	+VCC1.05_OUT_FET	To +VCCST_CPU
T8	+1.8V_PRIM_PG	To +VCCIN_AUX
T9	+VCCIN_AUX	To +VCCIN_AUX_VR_PG
T10	+VCCIN_AUX_VR_PG	To PCH_RSMRST#
T11	PCH_RSMRST#	To ESP_RESET#
T12	ESP_RESET#	To AC_PRESENT
T13	AC_PRESENT	To SIO_SLP_S4#
T14	SIO_SLP_S4#	To SIO_SLP_S5#
T15	SIO_SLP_S5#	To CPU_C10_GATE#
T16	SIO_SLP_S4#	To SIO_SLP_S0#
T17	SIO_SLP_S4#	To RUN_ON_EC
T18	SIO_SLP_S4#	To +1.1V_MEM
T19	SIO_SLP_S4#	To +0.6V_VDDQ
T20	SIO_SLP_S4#	To +1.8V_MEM
T21	SIO_SLP_S4#	To +1.8V_MEM
T22	SIO_SLP_S4#	To +VCC1P8A
T23	SIO_SLP_S4#	To +VCC_SFR_OC
T24	SIO_SLP_S4#	To +3VS
T25	RUN_ON_EC	To +1.8VS
T26	RUN_ON_EC	To +5VS+5VBS
T27	RUN_ON_EC	To -3.3VDD_SSD
T28	RUN_ON_EC	To -3.3VDD_SSD
T29	RUN_ON_EC	To -SSD_PWR#
T30	RUN_ON_EC	To -SSD_PWR#
T31	-3VS	To RUNPWROK
T32	RUNPWROK	To BVP_VR_ON_P
T33	BVP_VR_ON_P	To +VCCIN
T34	+VCCIN	To PCH_PWRK_P
T35	PCH_PWRK_P	To CPU_PWRGD
T36	CPU_PWRGD	To SYS_PWRK
T37	SYS_PWRK	To PCH_PLTRST#_EC

Power Down Sequence

EC pay attention timing

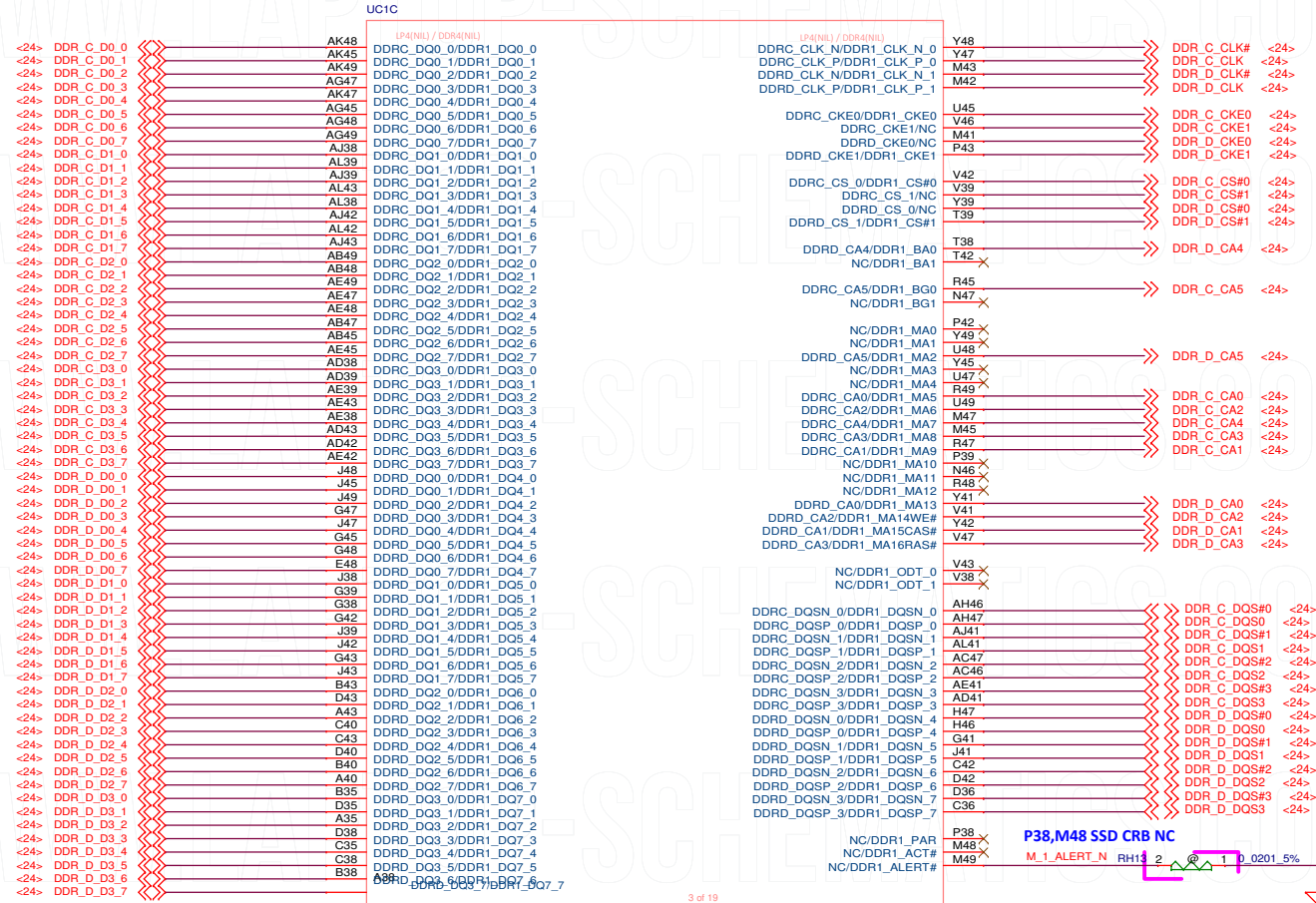


Memory connection refer 573975 Rev1P1



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								Size		Document Number		Rev	
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Memory connection refer 573975 Rev1P1



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								Size		Document Number	
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								Date:		Tuesday, December 24, 2019	
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										0.1 (X00)	

ESPI OR EC LESS

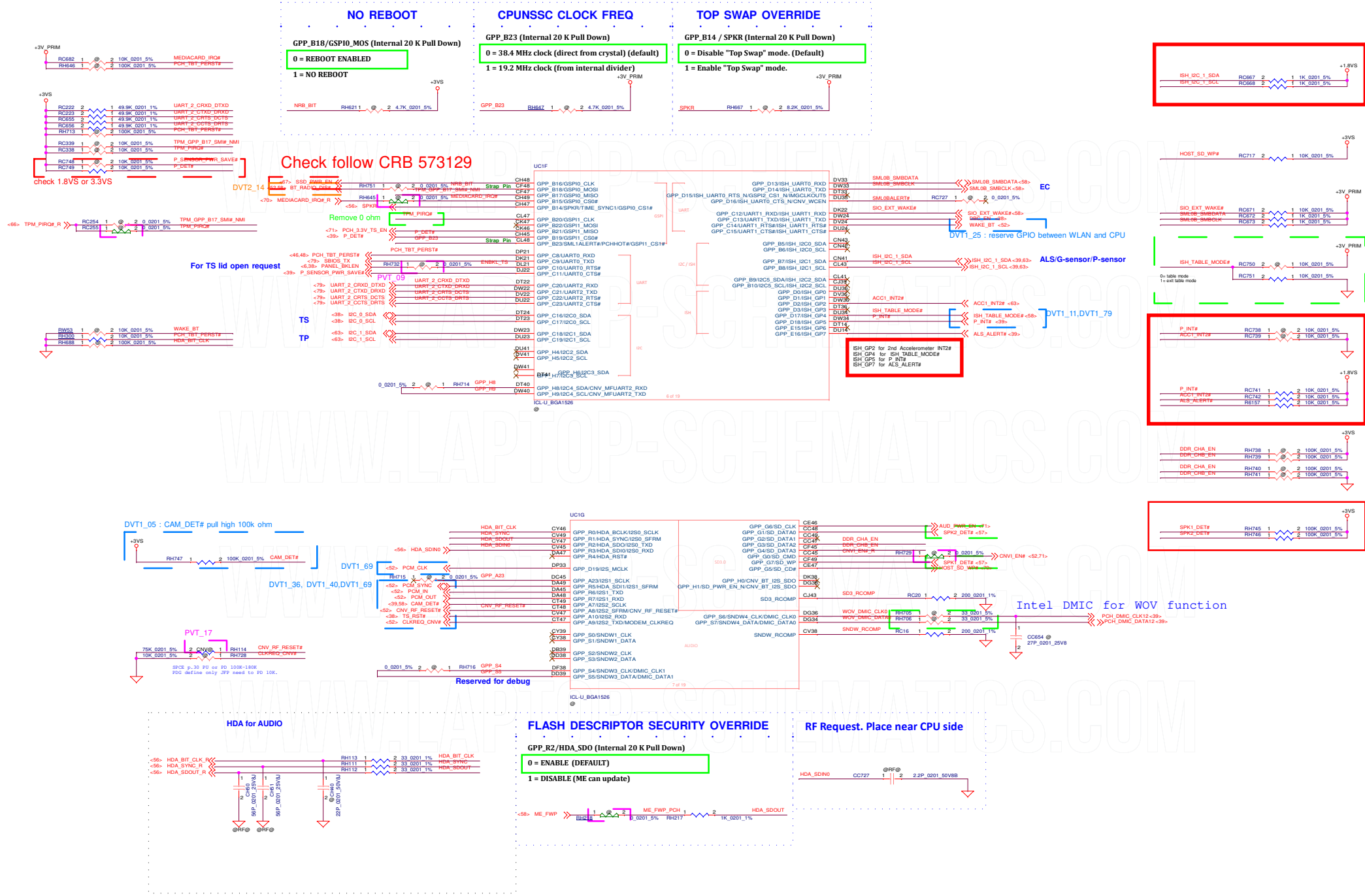
GPP_C5 (Internal 20 K internal Pull Down): SML0ALERT#

0 = Enable eSPI. (Default)

1 = Disable eSPI.



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3V SELECT STRAP

INPUT3VSEL

0 = 3.3V +/-5%

1 = 3.0V +/-5%



STRAP FOR SPI 1.8V/3.3V SEL

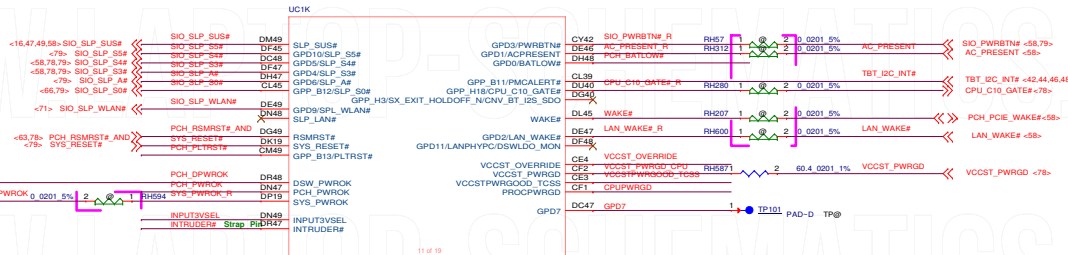
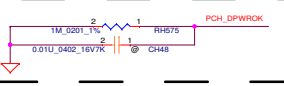
INTRUDER#

0 = SPI voltage is 3.3V

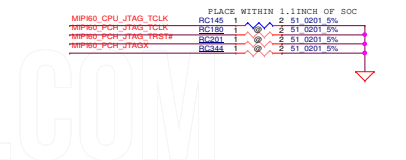
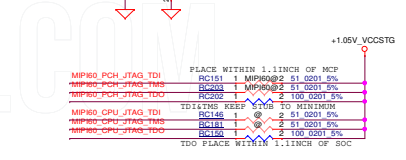
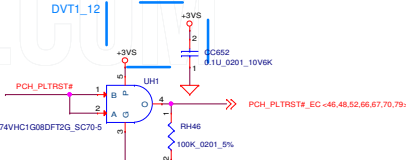
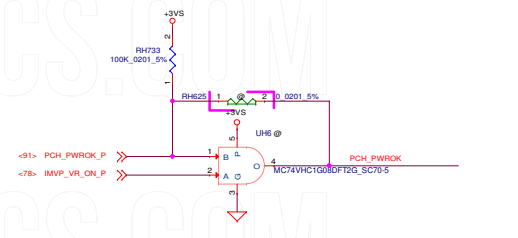
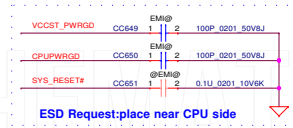
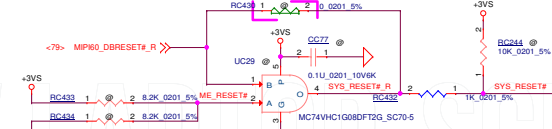
1 = SPI voltage is 1.8V



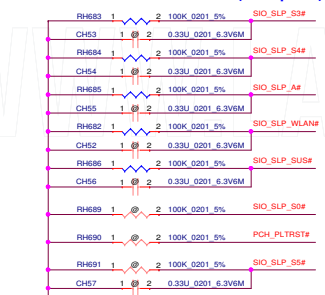
Microchip suggest 100K on RH575



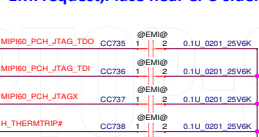
if pop UC29, RC244 also need pop



PCH GLITCH ISSUE MITIGATION(PDG p.306)



EMI request, Place near CPU die.

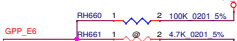


JTAG ODT DISABLE

GPP_E6

0 = JTAG ODT DISABLED

1 = JTAG ODT ENABLED

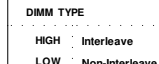
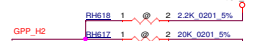


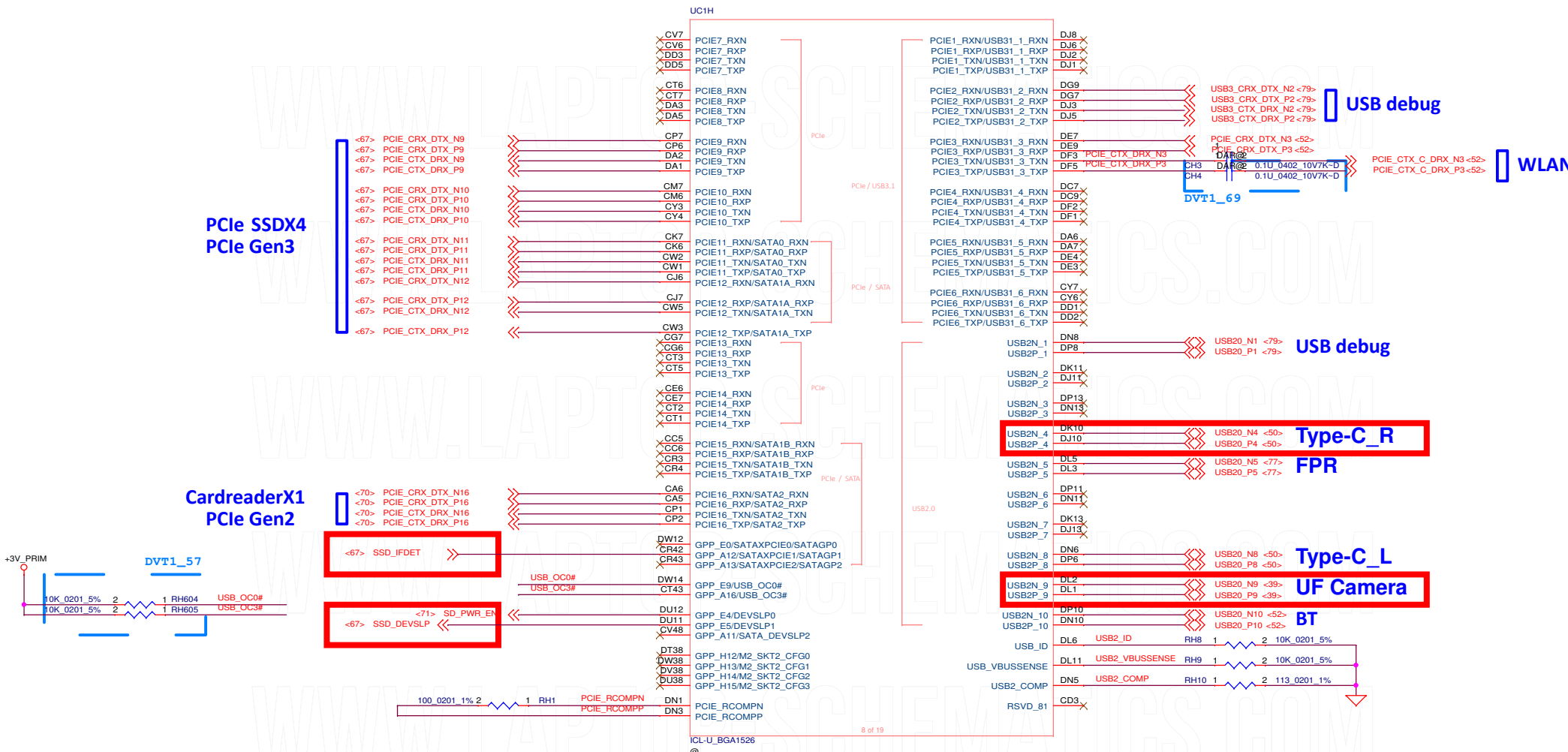
MAF/SAF STRAP(eSPI Flash Sharing Mode)

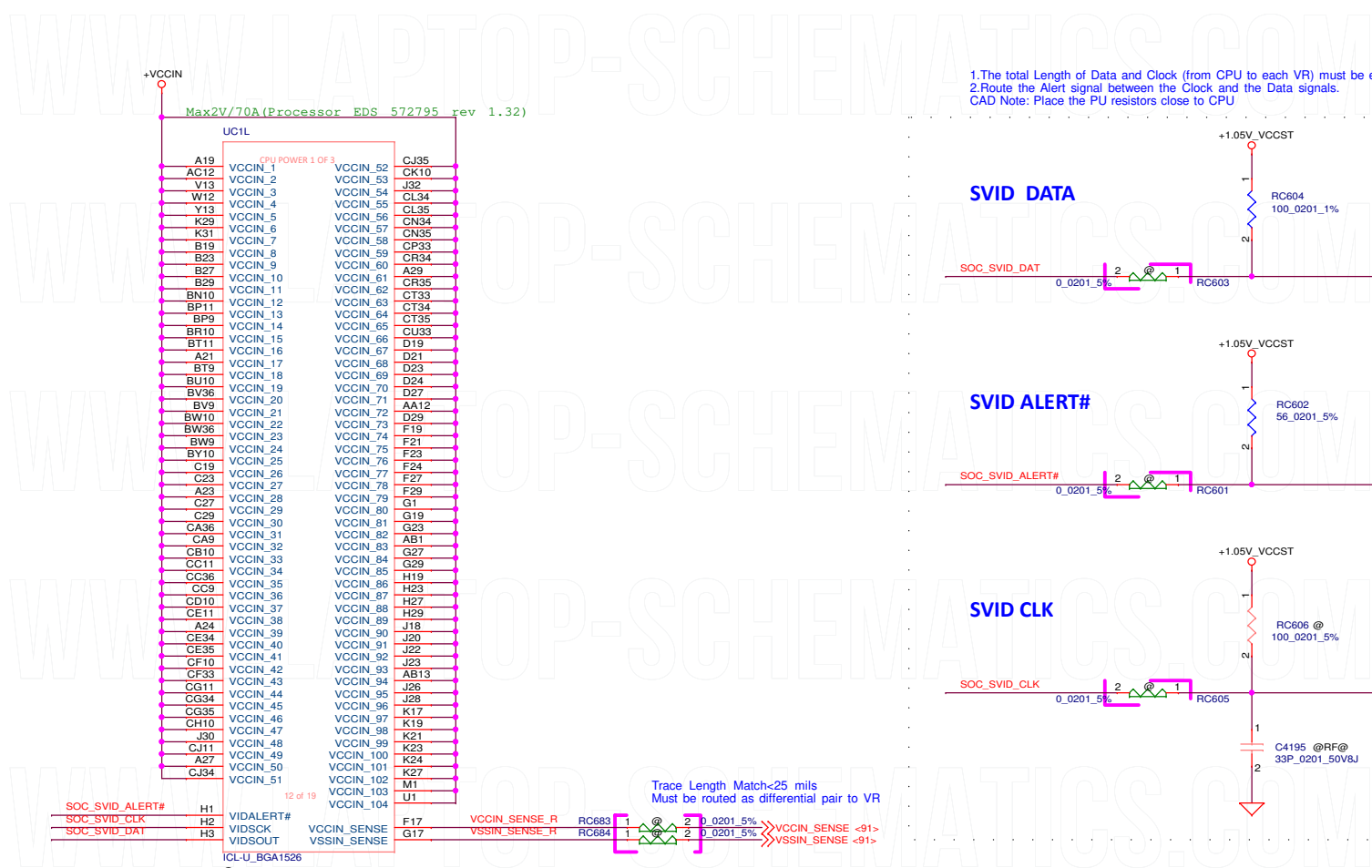
GPP_H2/CNV_BT_I2S_SDI(INTERNAL PD 20K)

0 = MAF (Master Attached Flash)

1 = SAF (Slave Attached Flash)

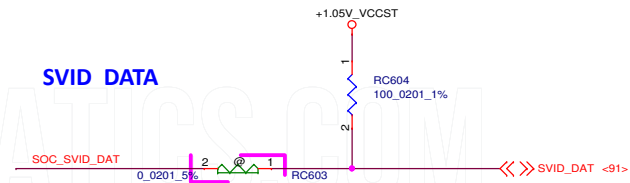




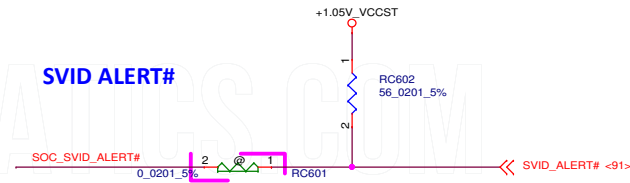


1.The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2.Route the Alert signal between the Clock and the Data signals.
CAD Note: Place the PU resistors close to CPU

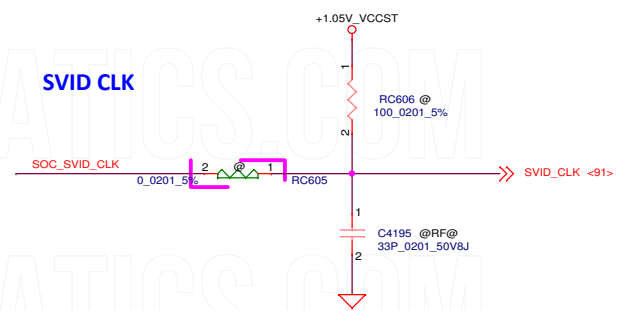
SVID DATA



SVID ALERT#

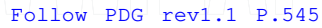


SVID CLK

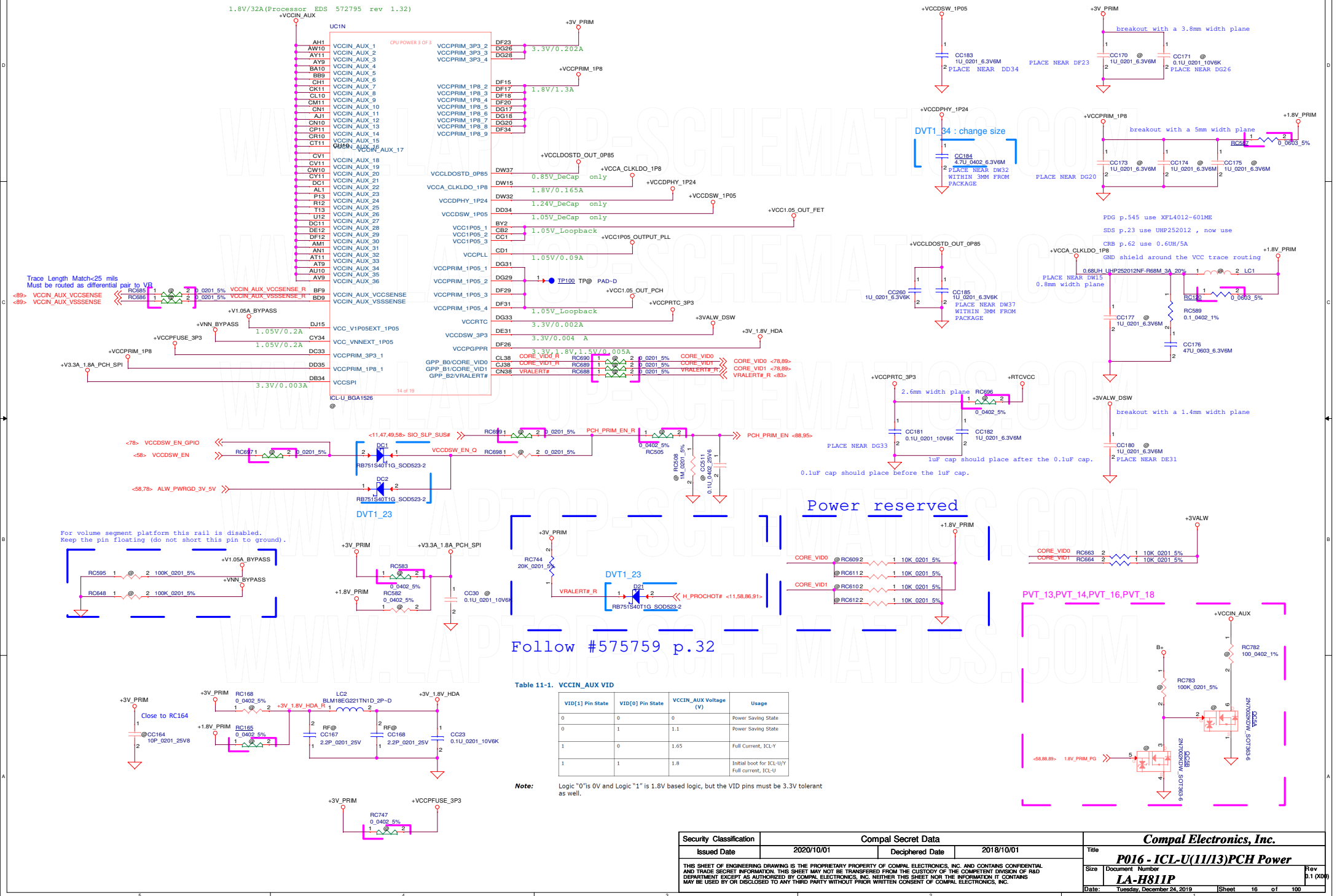


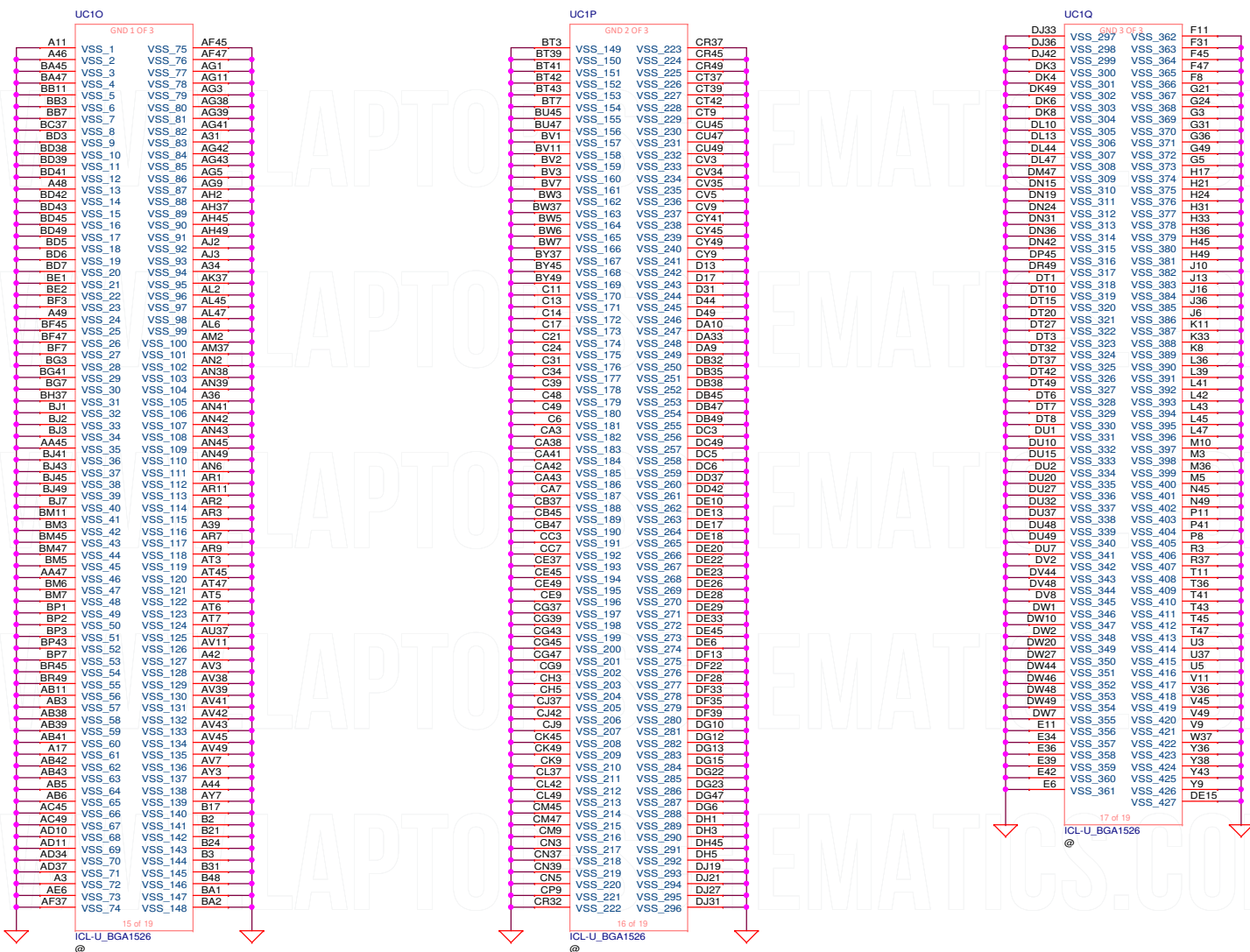
Trace Length Match<25 mils
Must be routed as differential pair to VR

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				Size	Document Number	Rev
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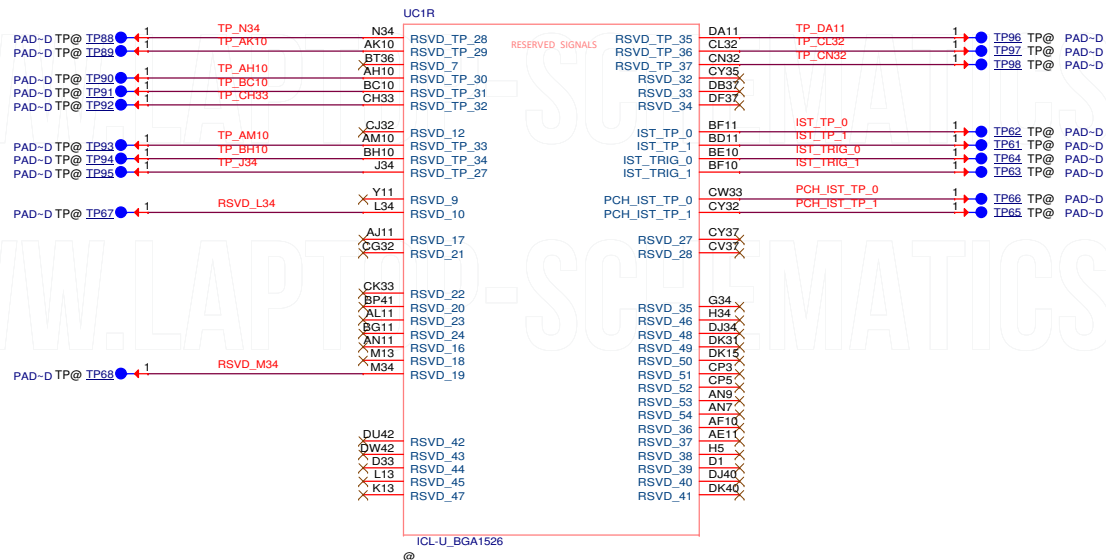
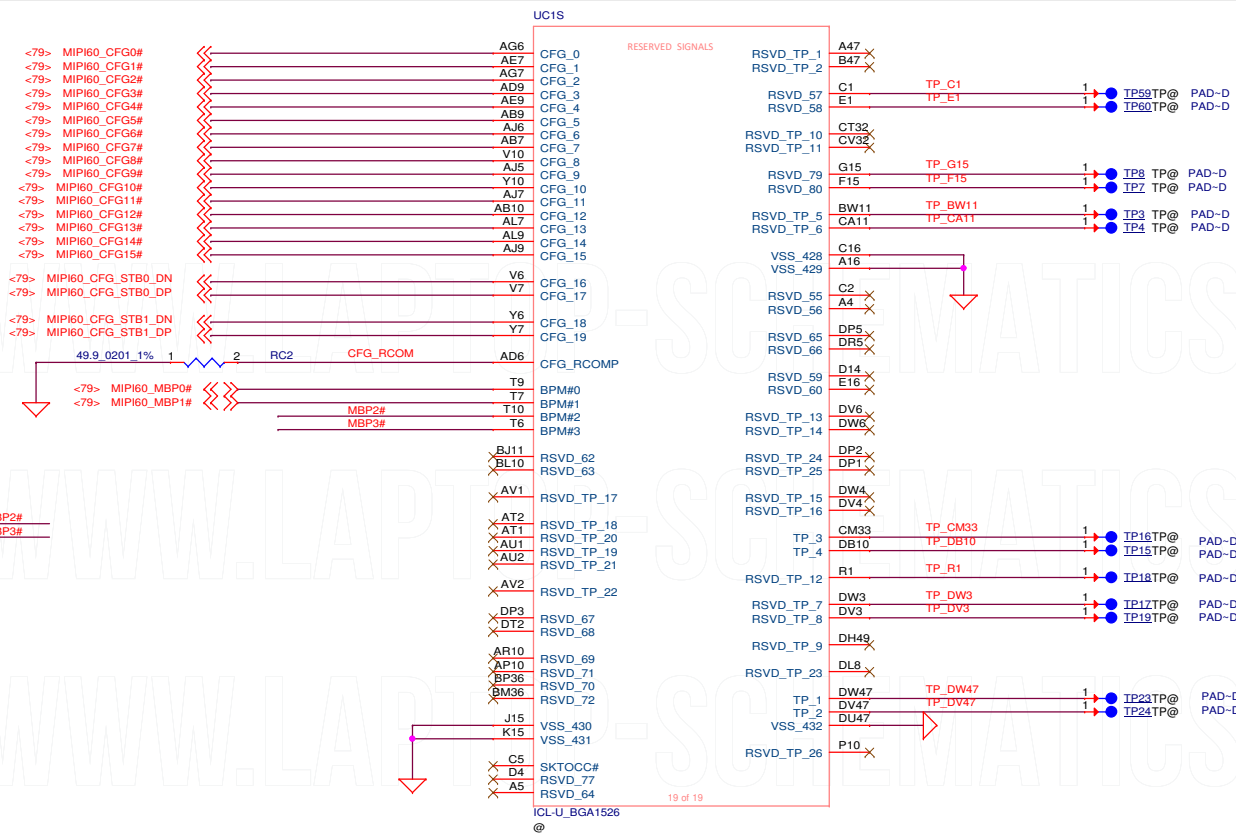




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+VCCIO_OUT

RC723 1 @ 2 10K 0201.5% MBP2#
RC724 1 @ 2 10K 0201.5% MBP3#



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					P019 - Reserve		
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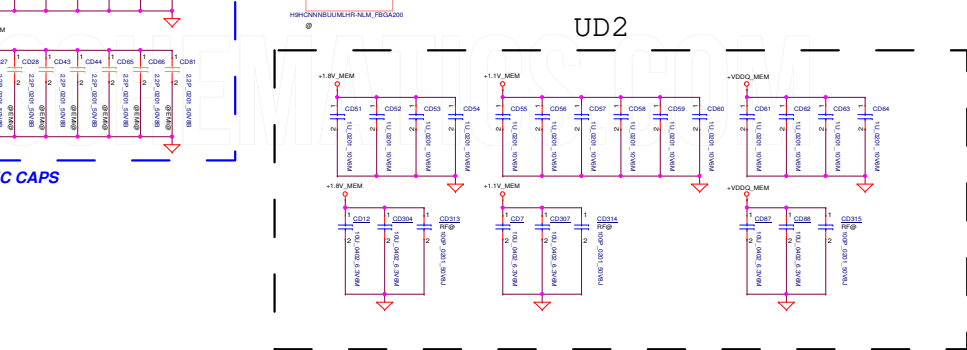
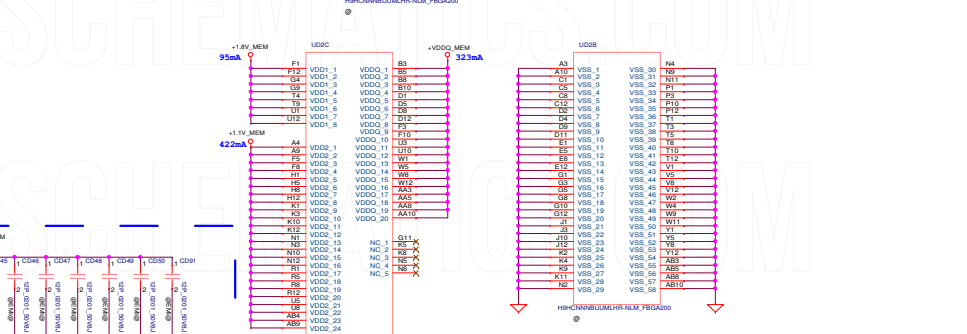
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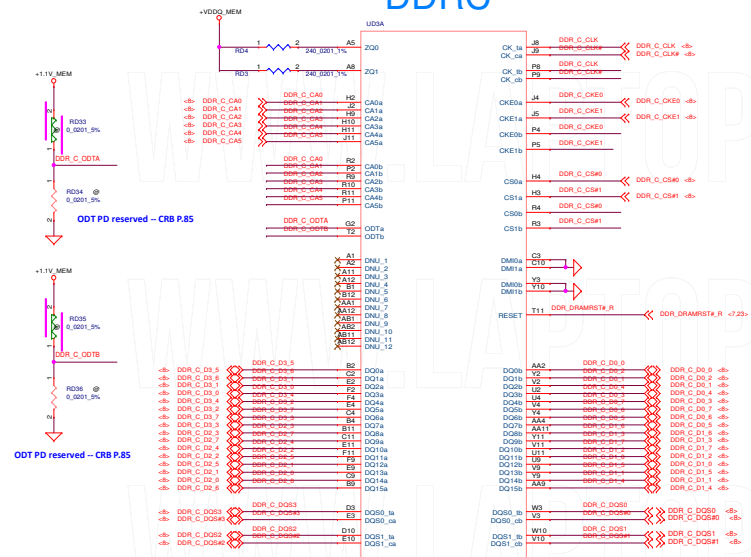
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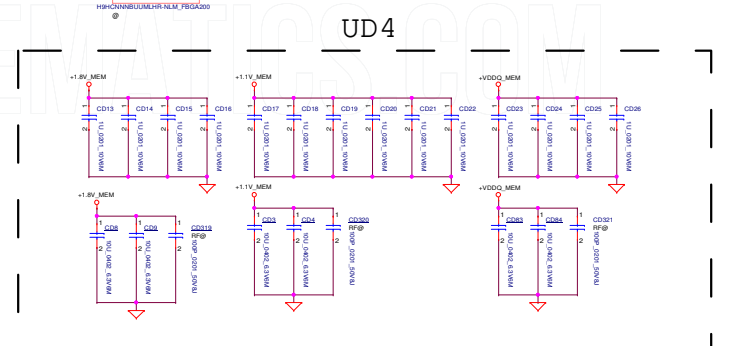
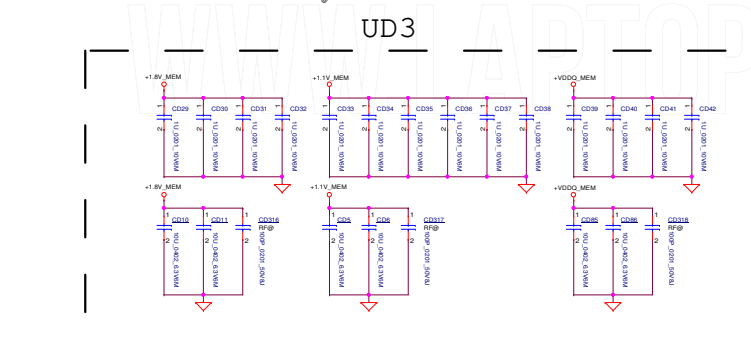
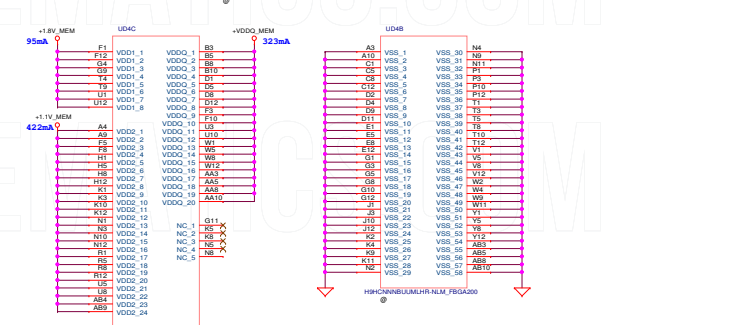
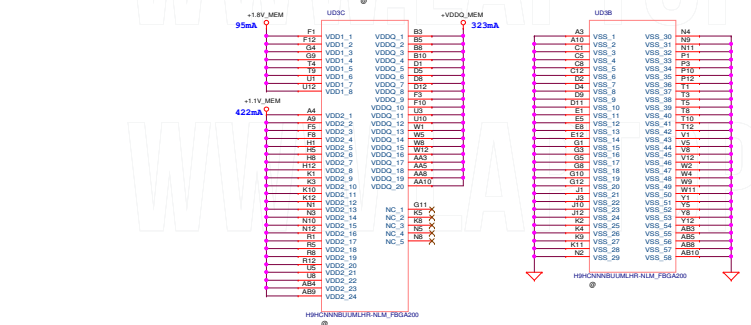


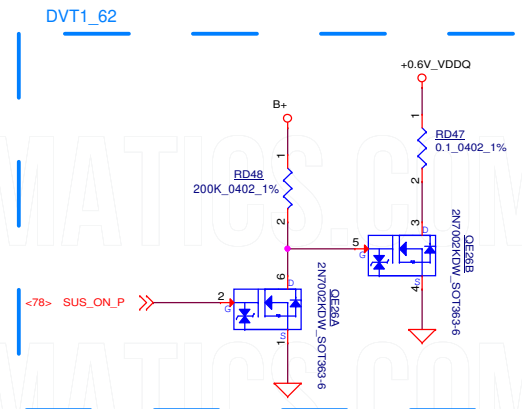
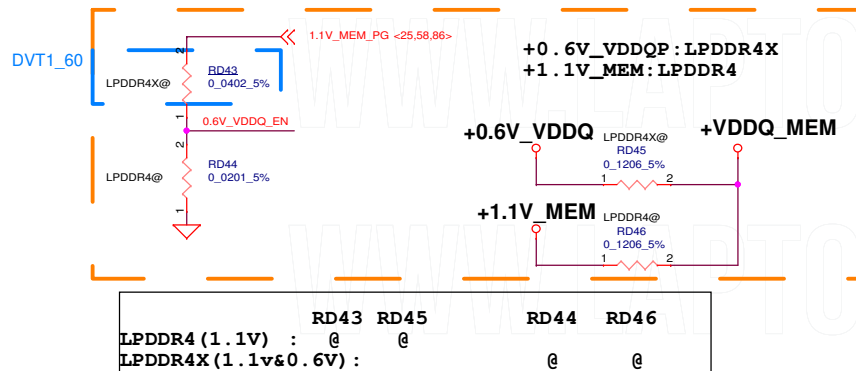
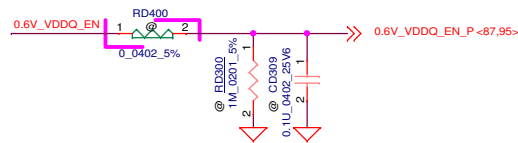
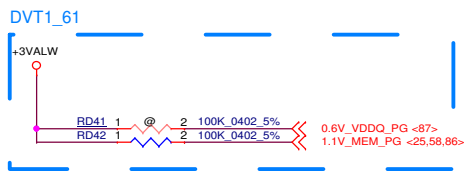
Memory connection refer 573975 Rev1P1

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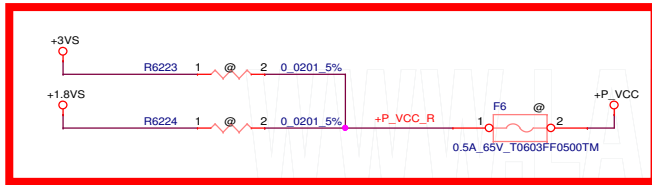
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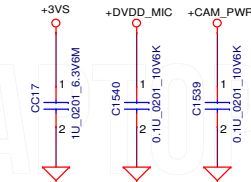
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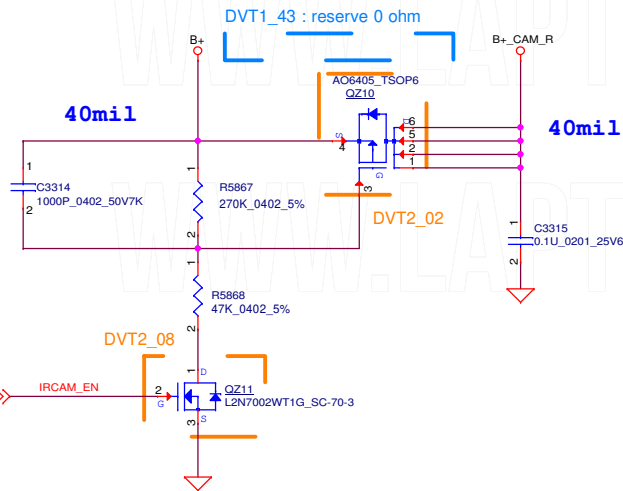
For factory test request



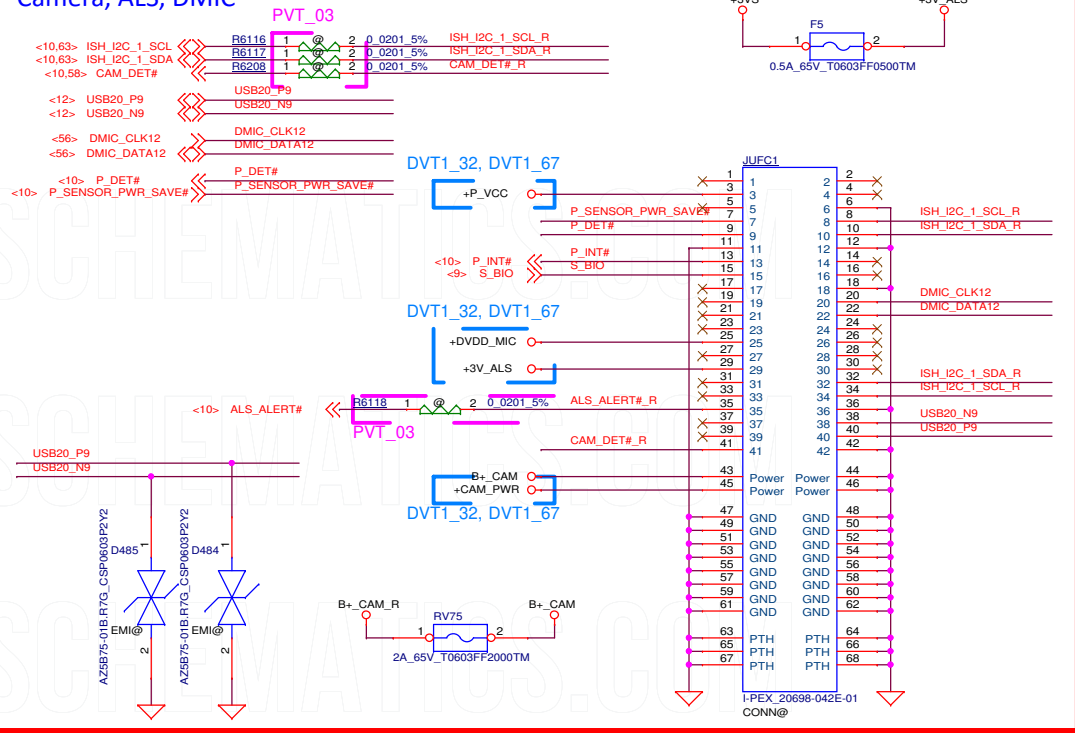
Bypass cap close to CONN



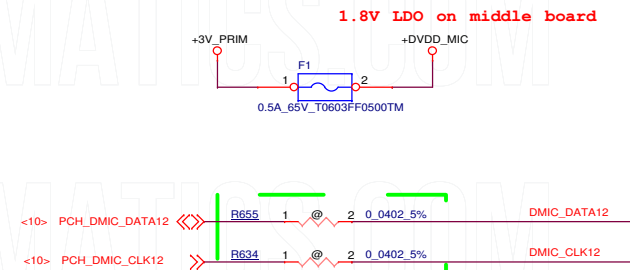
DVT1_20, DVT1_67



Camera, ALS, DMIC

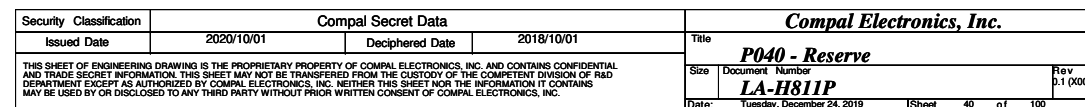


Intel DMIC for WOV function



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DVT1 16 : add Darwin2.0



Pin1 : +3V
Pin2 : GND
Pin3 : XRS
Pin4 : SWD_CLK
Pin5 : SWD_DAT

The diagram illustrates the hardware connections for the Darwin2.0 system. Key components and their connections are as follows:

- Pin Header (Green Box):**
 - Pin1 : +3V
 - Pin2 : GND
 - Pin3 : XRS
 - Pin4 : SWD_CLK
 - Pin5 : SWD_DAT
- IceLake-U 4+2 (p.52):**
 - Connected to **WLAN** via I2S and UART.
 - Connected to **EC** via SMBUS.
- EC (p.58):**
 - Connected to **MCU** via GPIO111, GPIO126, GPIO121, and I2C1.
 - GPIO111 is connected to the **INT#** pin of the MCU through a 0-ohm resistor and a 100K-ohm pull-up to +3VALW.
- WLAN (p.52):**
 - Connected to **MCU** via UART.
- MCU (p.40):**
 - Connected to **P-Sensor** via I2C.
 - Connected to **DEG CONN** via I2C.
 - Connected to **JWLA1** (p.40) via CTRL2 and CTRL3.
 - Connected to **JWLA2** (p.40) via CTRL0 and CTRL1.
- Power and Grounding:**
 - +3VALW:** A 100K-ohm pull-up resistor connected to the MCU's INT# pin.
 - +3VS_WLAN_MCU:** A 100K-ohm pull-up resistor connected to the MCU's CTRL2 and CTRL3 pins.

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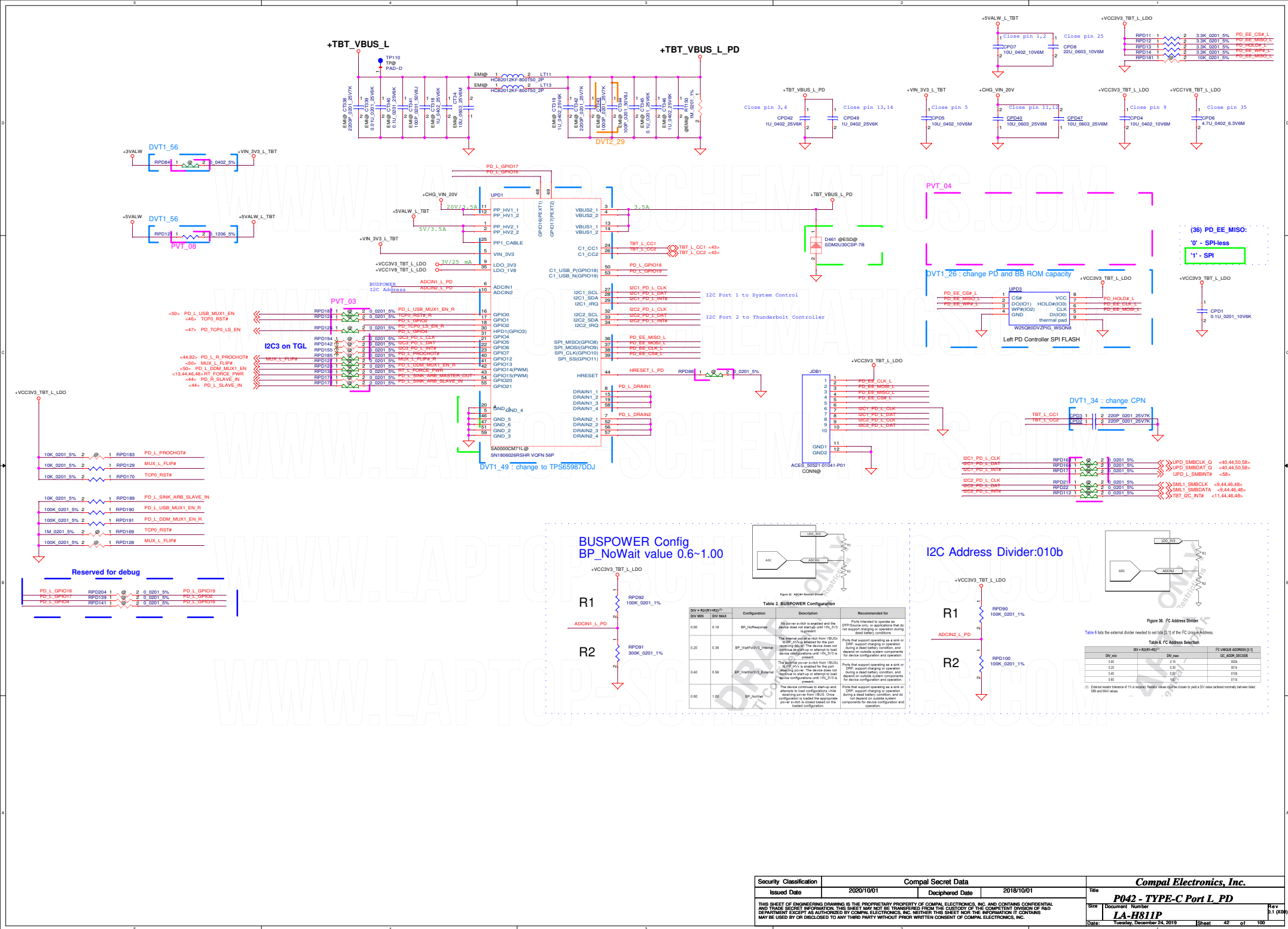
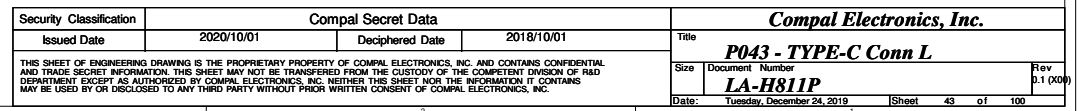
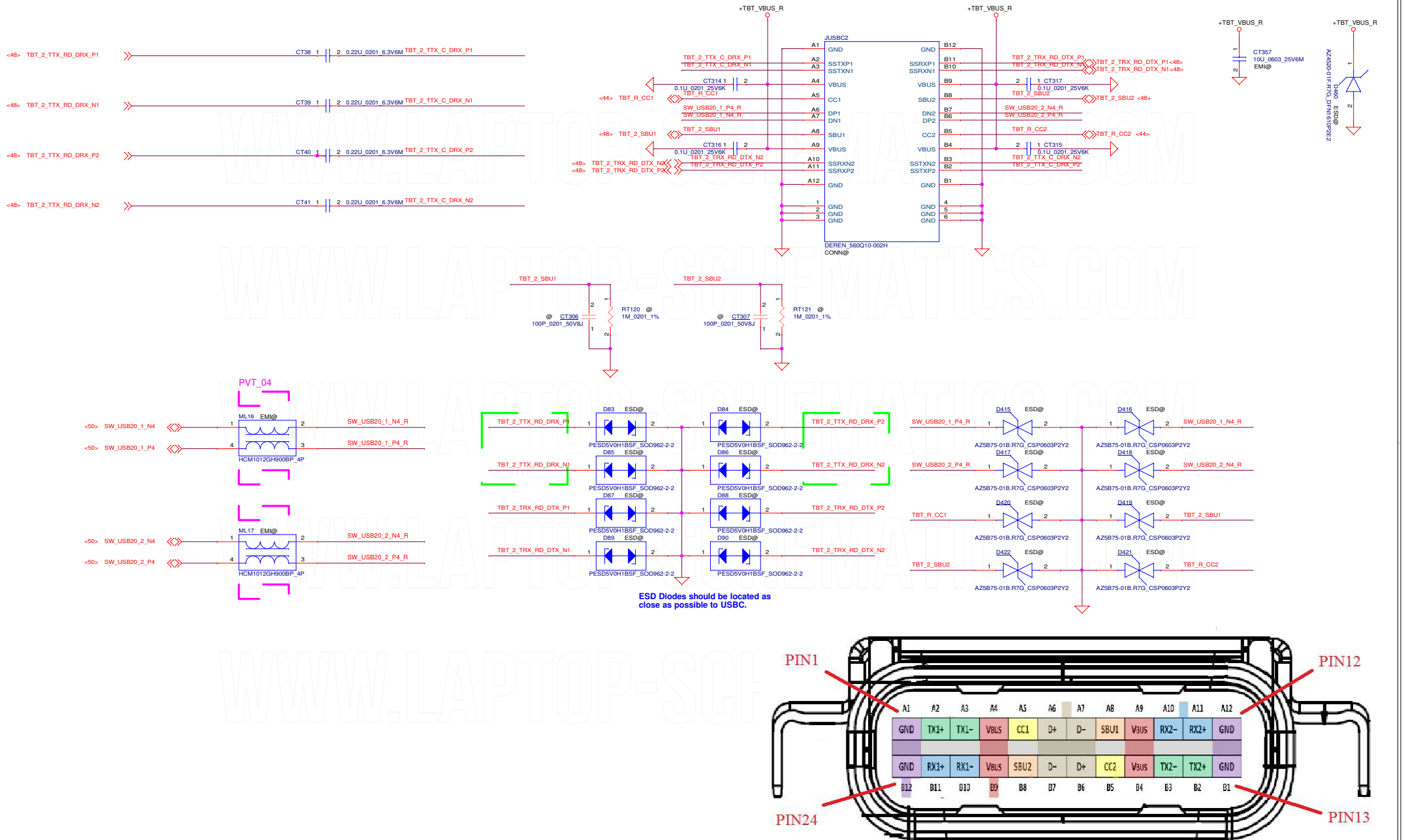


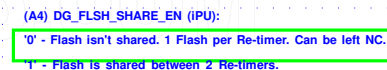
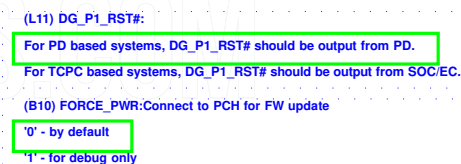
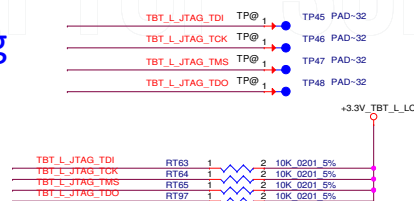
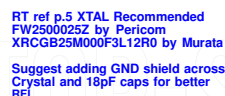
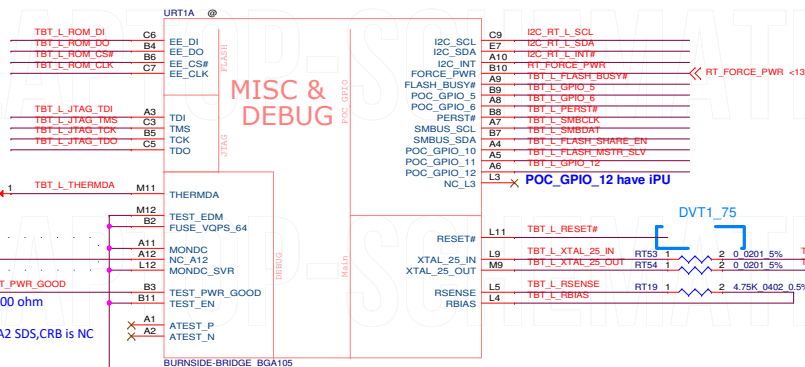
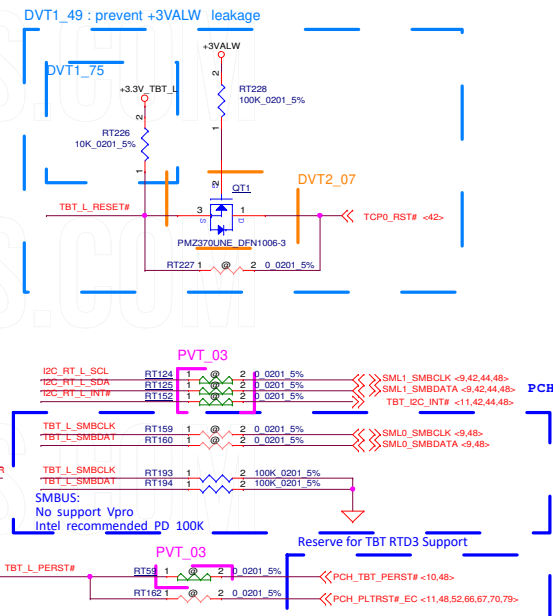
Diagram illustrating the pin configuration of the ADXL345 module. The module is a rectangular PCB with a central grid of pins. The pins are labeled A1 through A12 along the top edge, B1 through B12 along the bottom edge, and PIN1, PIN12, PIN13, and PIN24 at the corners. The central grid contains various pins including GND, TX1+, TX1-, VBUS, CC1, D+, D-, SBU1, VBUS, RX2-, RX2+, GND, GND, RX1+, RX1-, VBUS, SBU2, D-, D+, CC2, VBUS, TX2-, TX2+, and GND. Red lines connect the corner pins to their labels: PIN1 to A1, PIN12 to A12, PIN13 to B1, and PIN24 to B12.



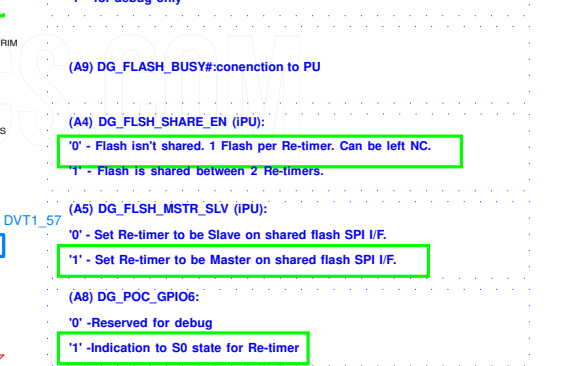
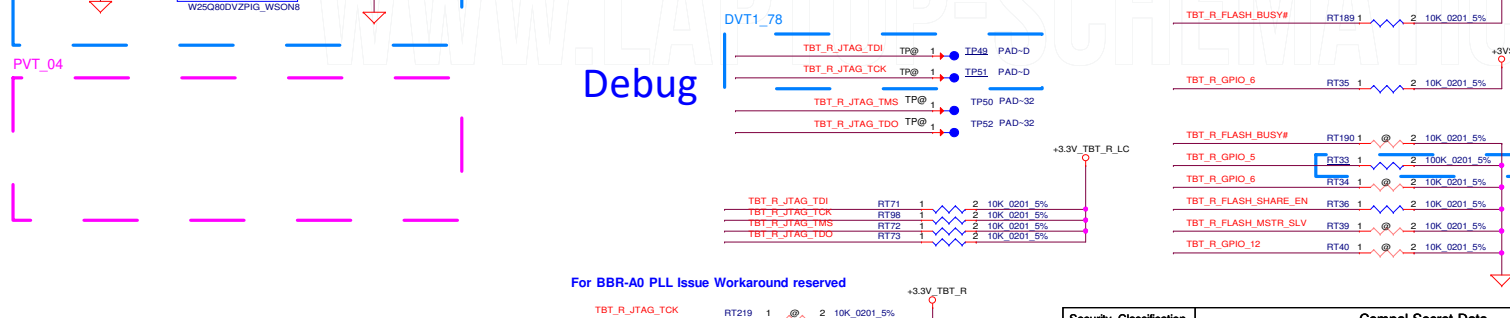
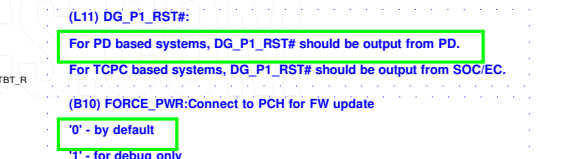
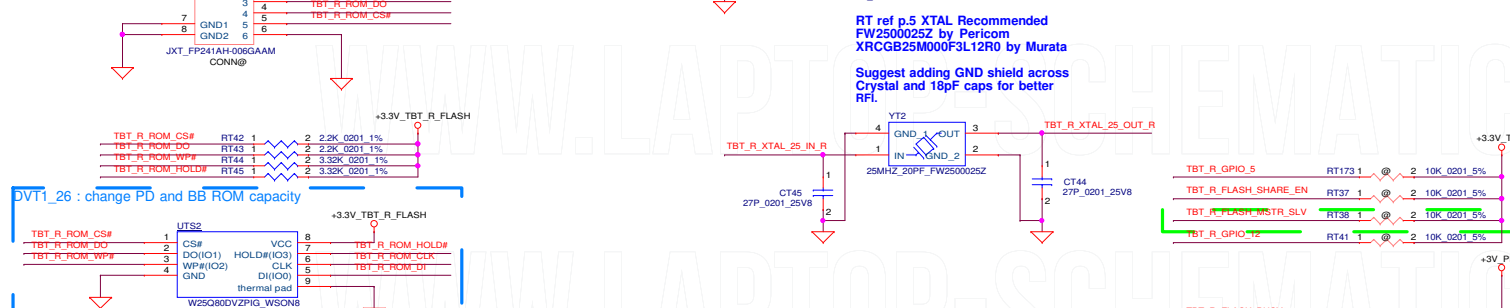
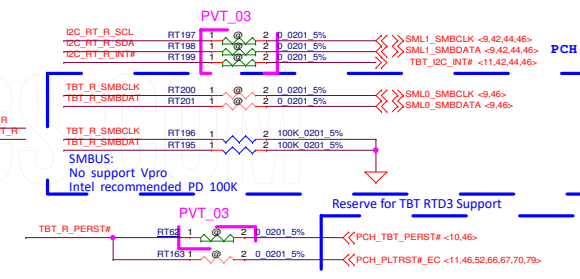
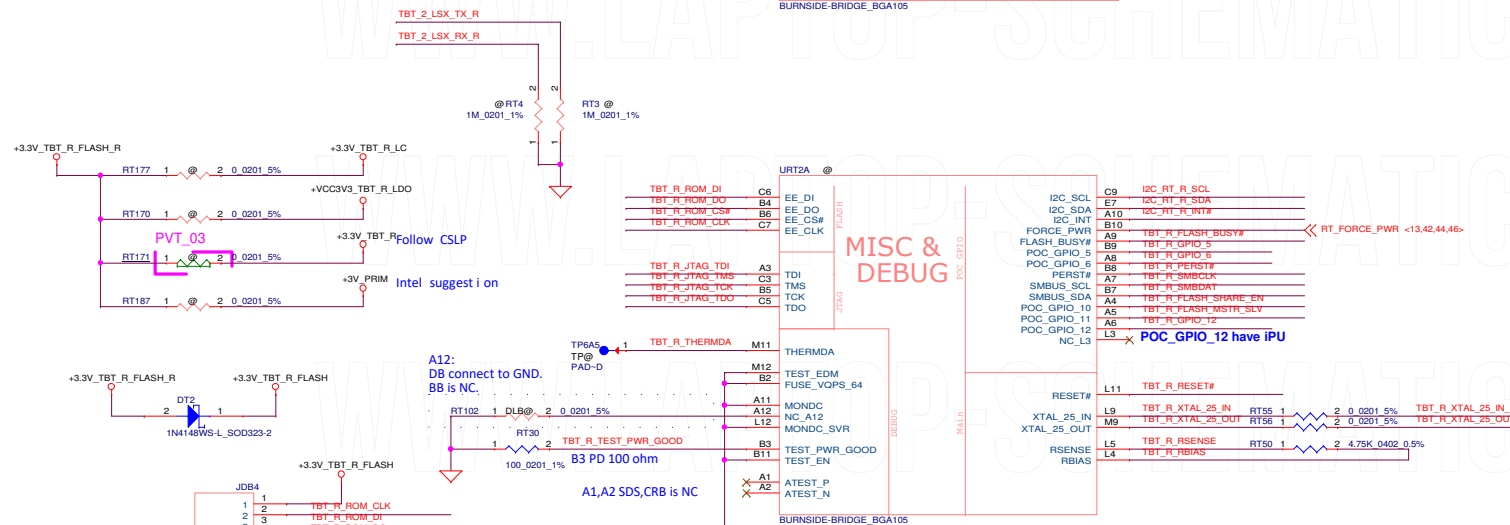
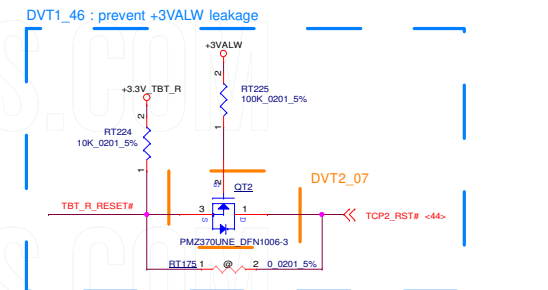
RIGHT Type-C Connector



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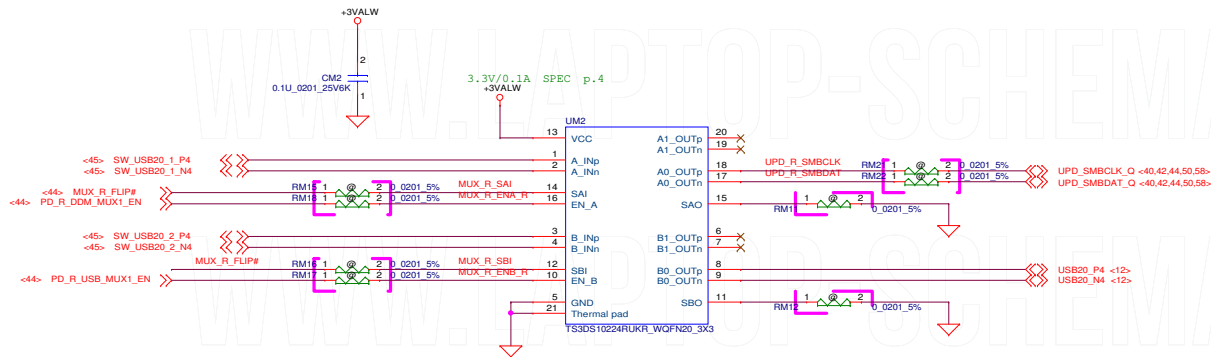
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For BBR-A0 PLL Issue Workaround reserved

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USB2/I2C MUXES_R



SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	—	INA	—
0001	INB	—	—	INA
0010	INB	—	INB	—
0011	INB	—	—	INB
0100	—	INB	INA	—
0101	—	INB	—	INA
0110	—	INB	INB	—
0111	—	INB	—	INB
1000	INA	—	INA	—
1001	INA	—	—	INA
1010	INA	—	INB	—
1011	INA	—	—	INB
1100	—	INA	INA	—
1101	—	INA	—	INA
1110	—	INA	INB	—
1111	—	INA	—	INB

					I2C	USB			
ENA	ENB	SAI	SBI	SAO	OUTA0	OUTB0	Mux	Functional Mode	PD Controller W/DDM
0	1	–	0	–	Hi-Z	BOT	–		USB only on TOP
0	1	–	1	–	Hi-Z	TOP	–		USB only on BOT
1	1	0	0	0	BOT	TOP	Crosspoint	Switch	USB on TOP W/DDM
1	1	1	1	0	TOP	BOT	Crosspoint	Switch	USB on BOT W/DDM

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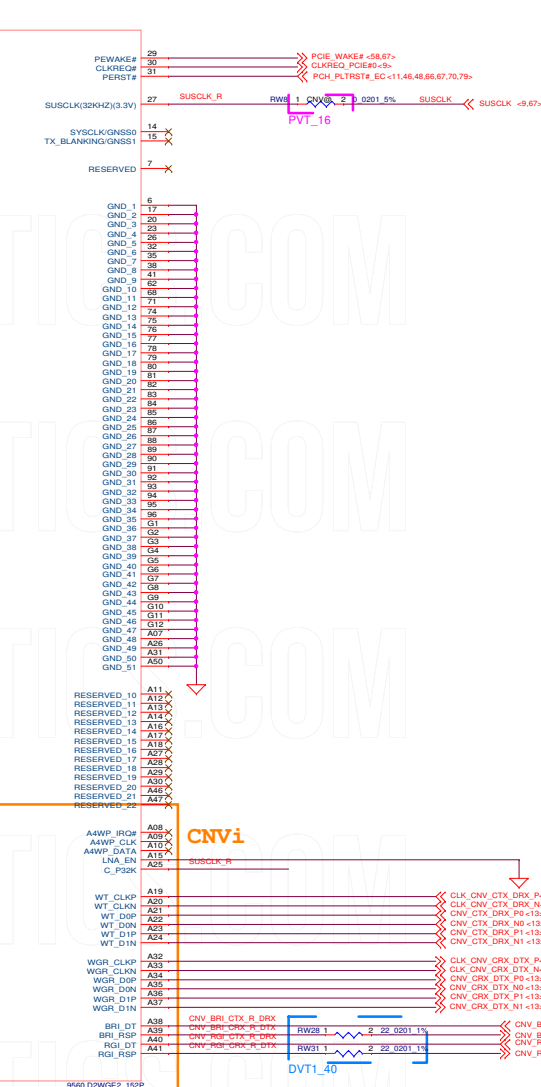
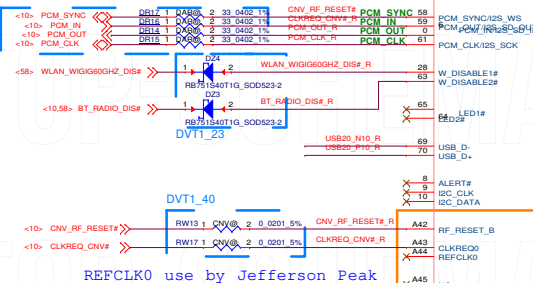
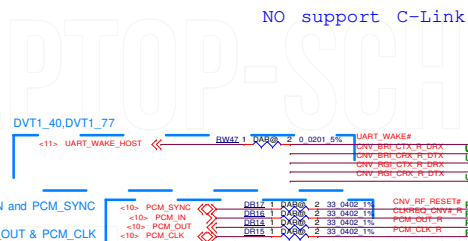
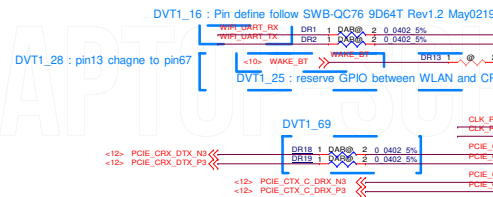
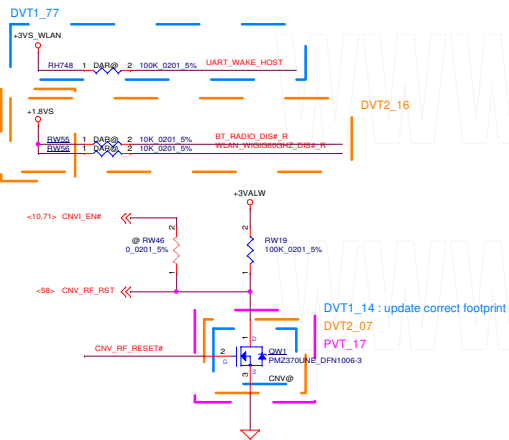
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DVT1_B1

+1.8VS PWR up sequence must be closed to +3VS_WLAN

DVT1_78

3.3V

1.8V

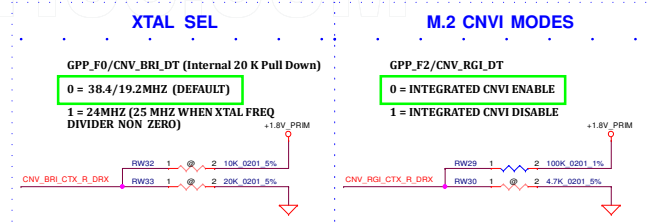
WIF1_UART_RX

DVT1_15

3.3V WLAN

1.8V

WIF1_UART_TX



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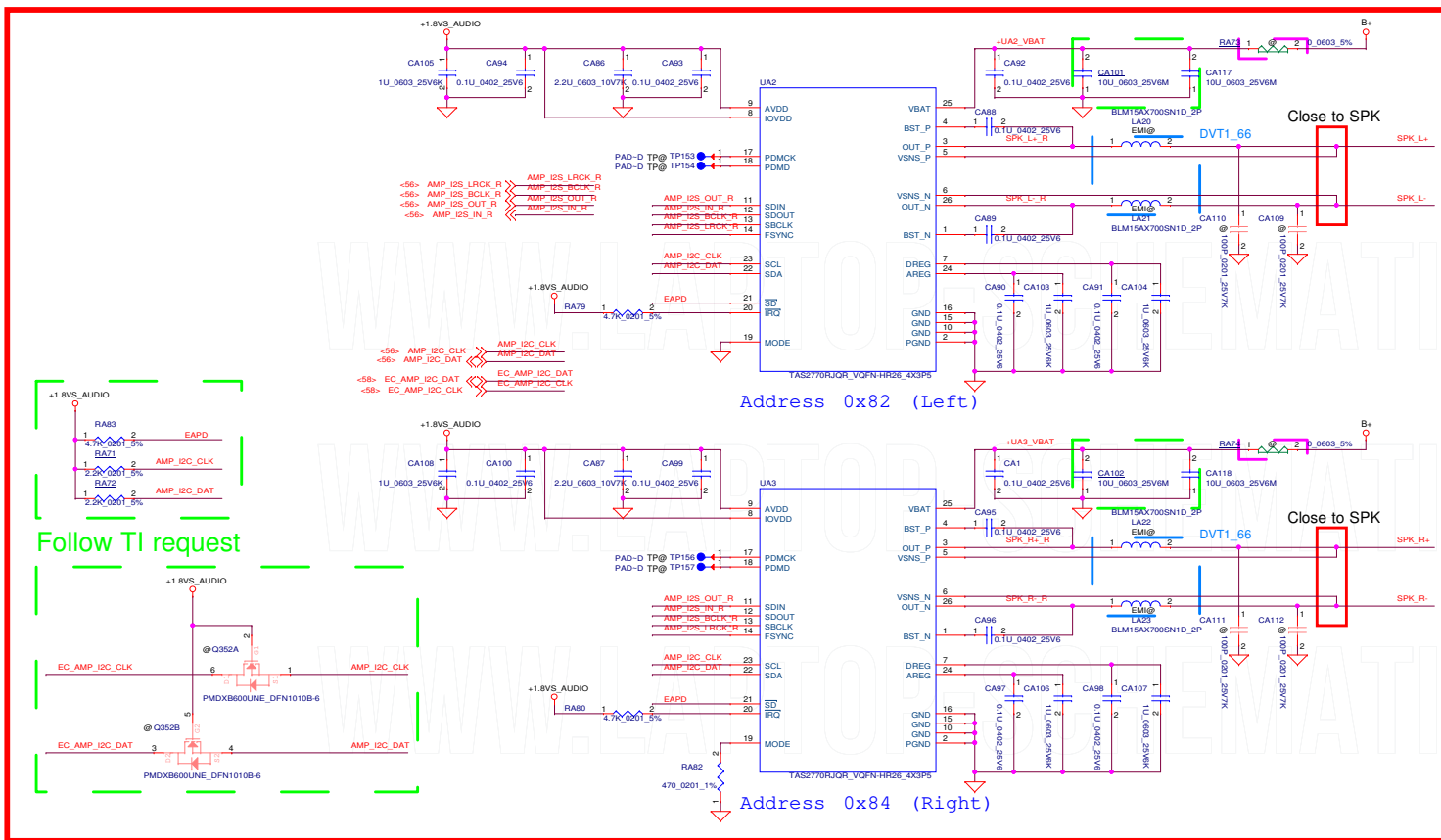
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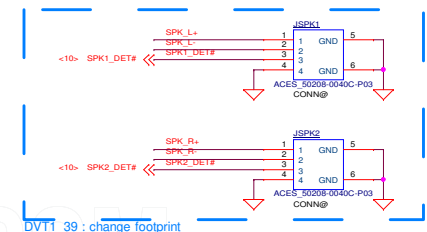
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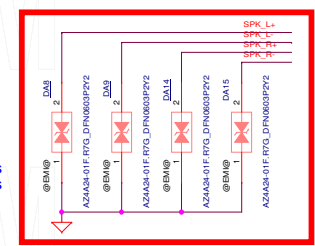
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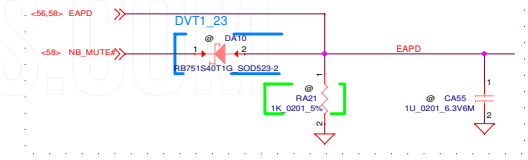
Int. Speaker Conn.



SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

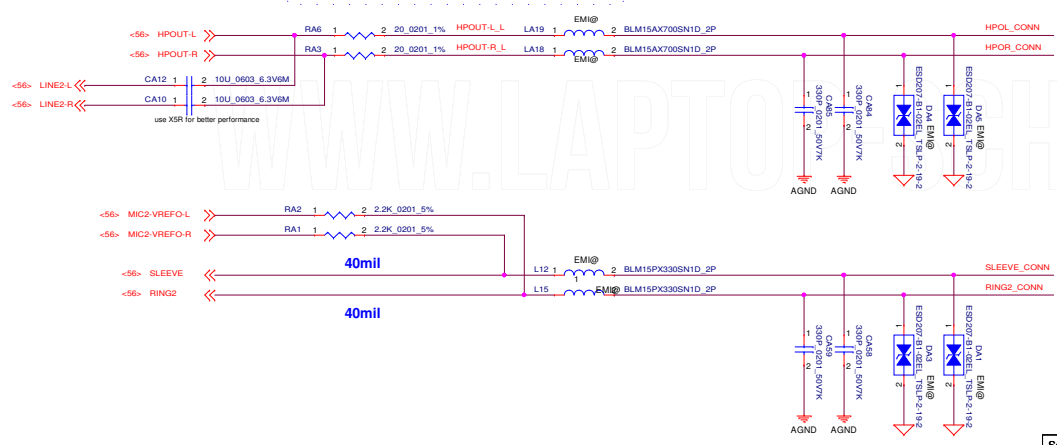


Need up to 15+V, check with EMC

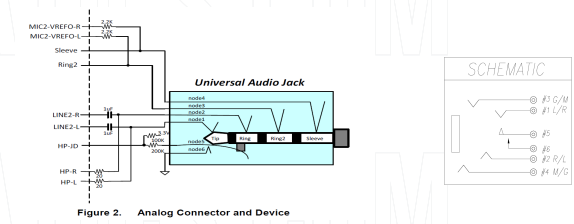


PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.
LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.
change RA6/RA3 to 5.6 ohm to meet Dell Grade A headphone output power > 25 mW setting

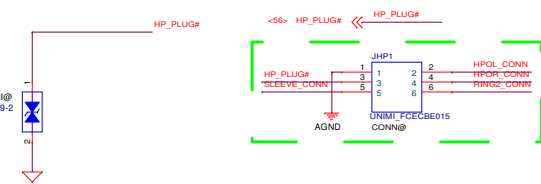
Universal Audio Jack



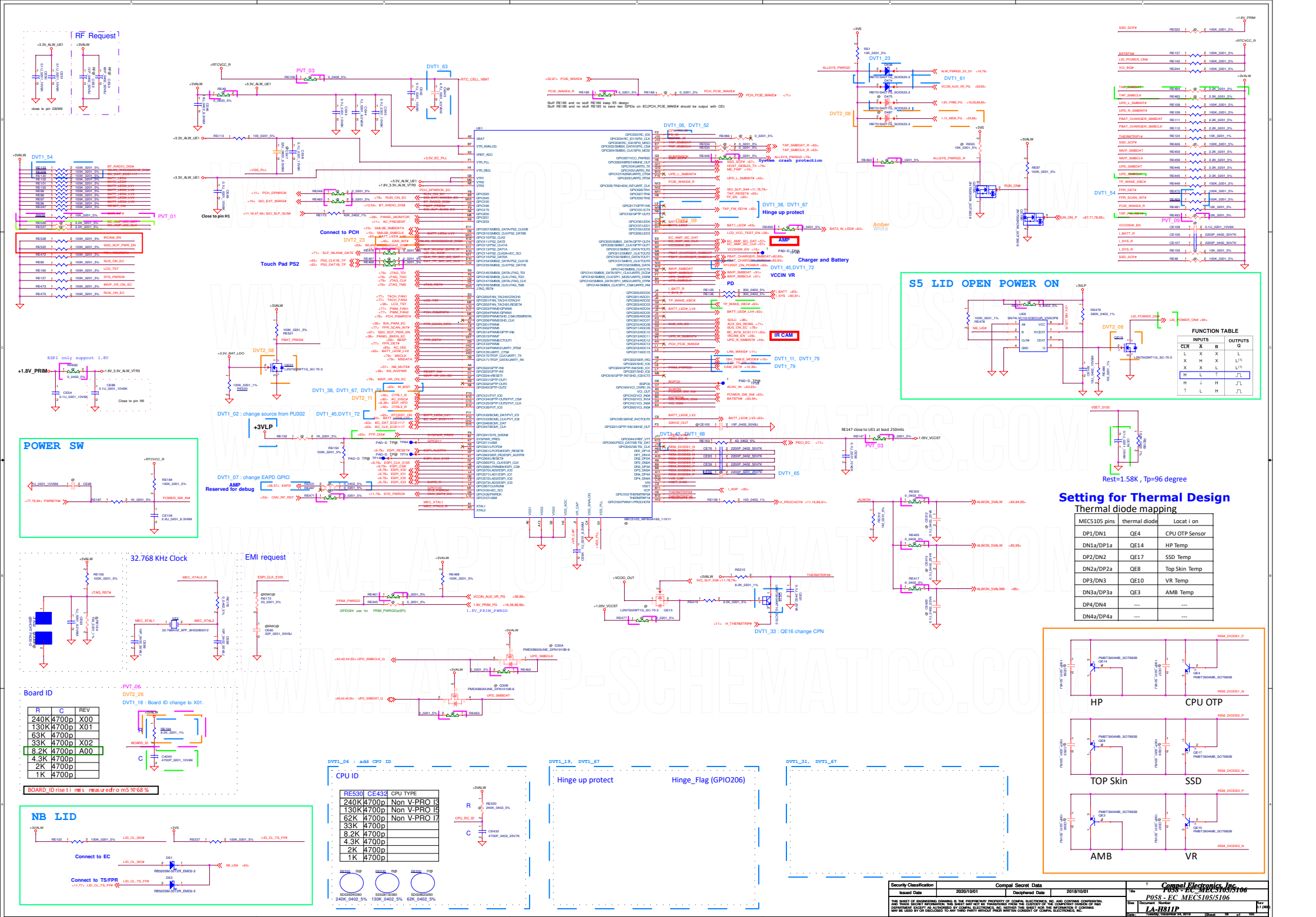
Universal Audio Jack CONN



Contact with PC BEAN



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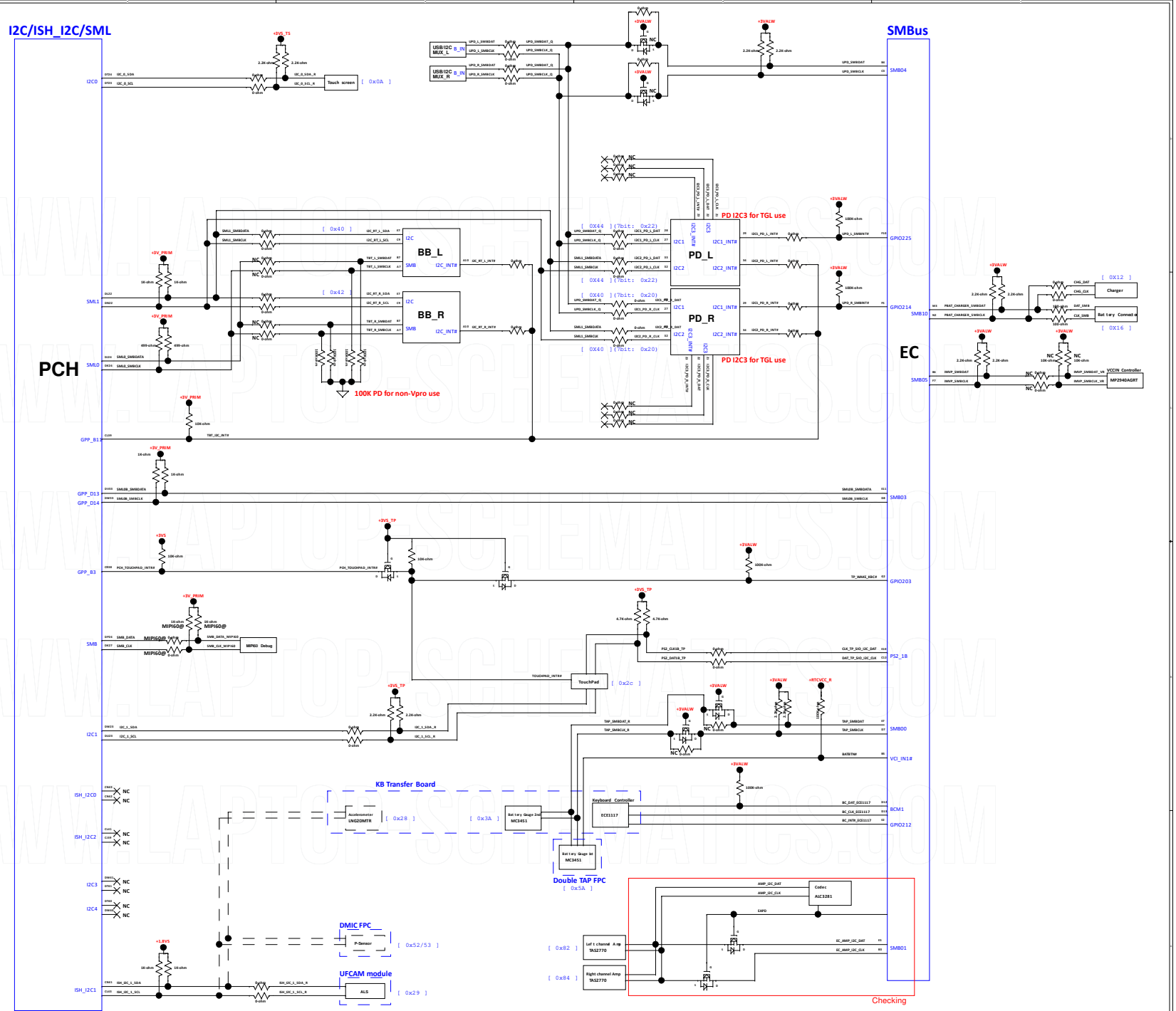
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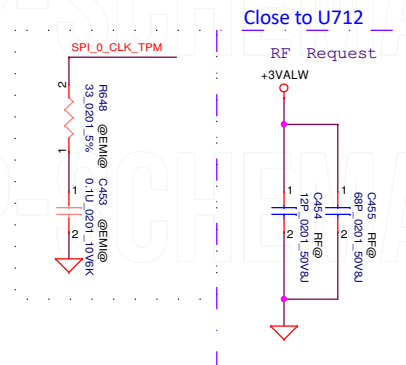
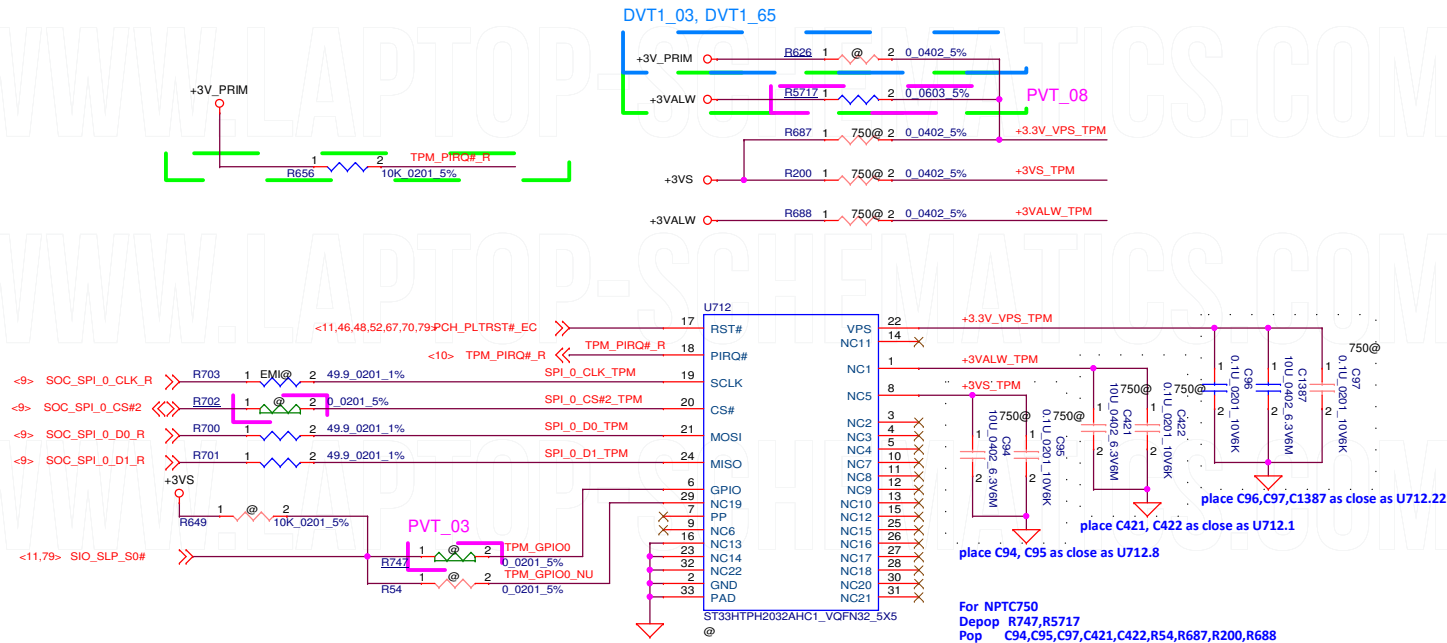
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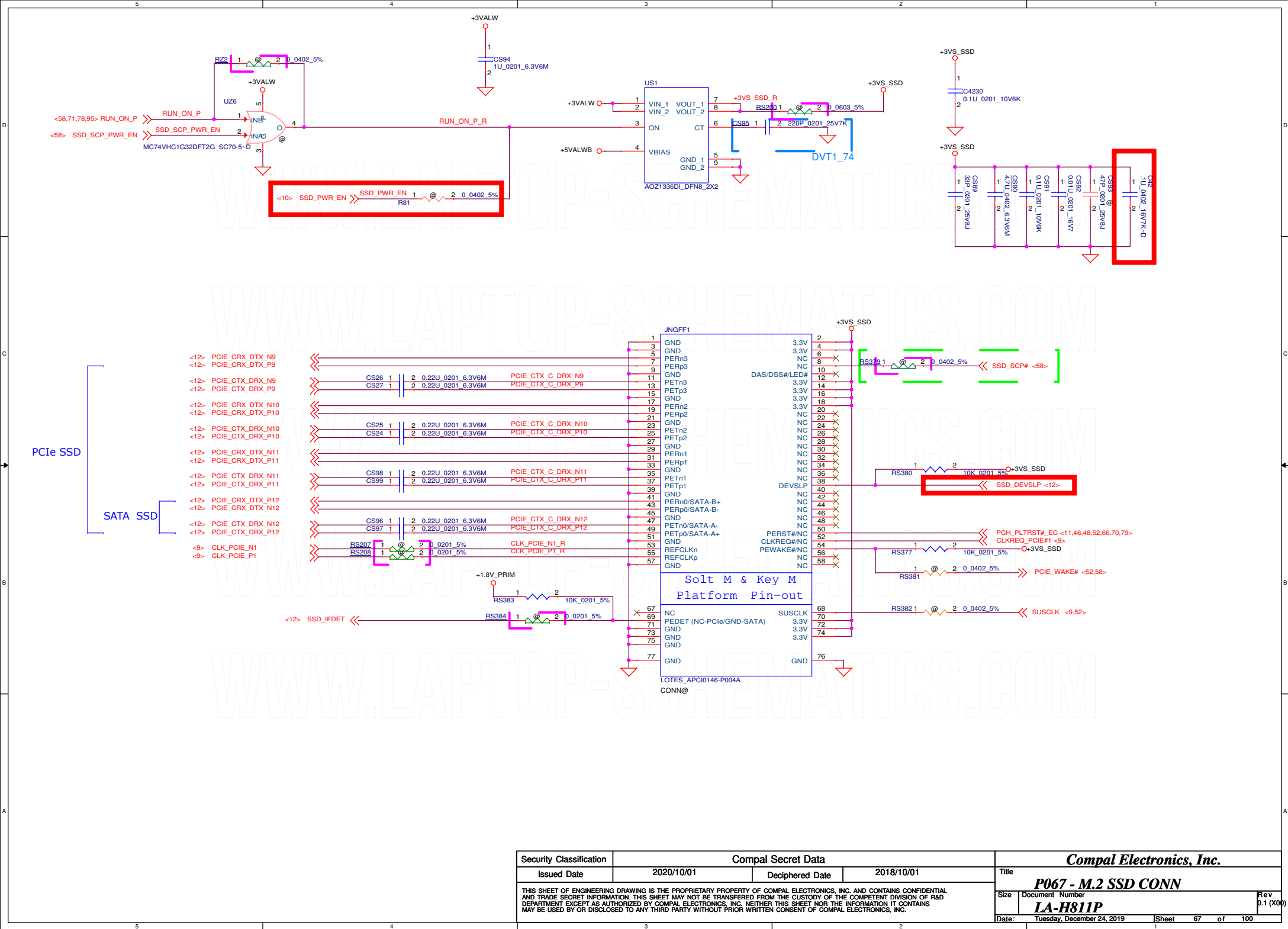
For ST/Nuvoton TPM



Pin number	1	2	6	8	16	17	18	19	20	21	22	23	24	29
Chip	1	2	6	8	16	17	18	19	20	21	22	23	24	29
ST33	NC	GND	GPIO0	NC	NC	RESET	PIRQ	SCLK	SCS	MOSI	VDD	NC	MISO	NC
NPTC750	VDD	NC	NC	RESET	GND	RESET	PIRQ	SCLK	SCS	MOSI	VDD	GND	MISO	GPIO0

VSB Standby Power Supply. The VALW power rail 3.3V
VHIO Host Interface Power Supply 3.3V
VPS: Power Supply 3.3V
NPTC750: GPIO0 can be used as a backup option for entering Low-Power mode.

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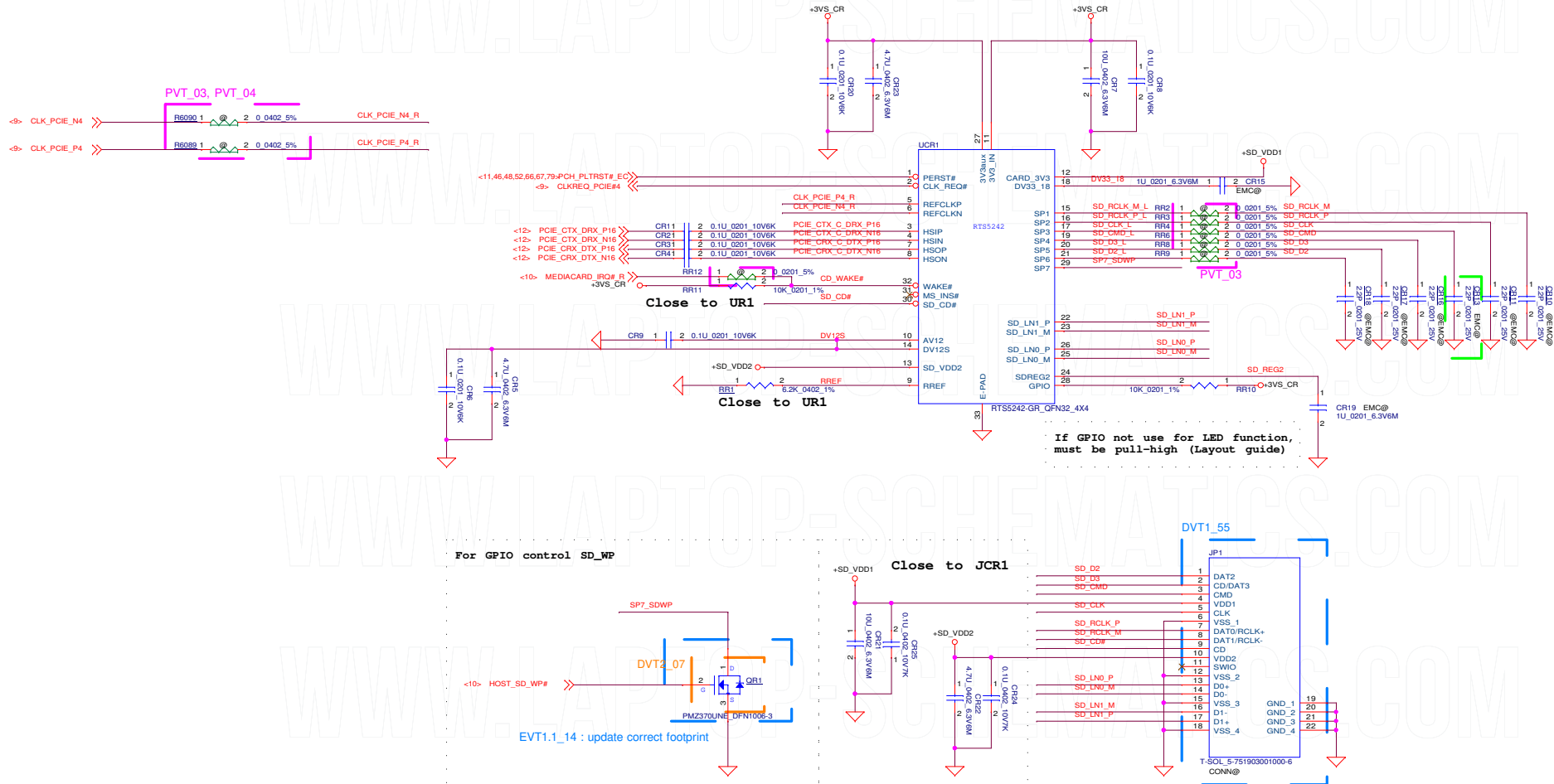
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Card Reader

- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card_3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



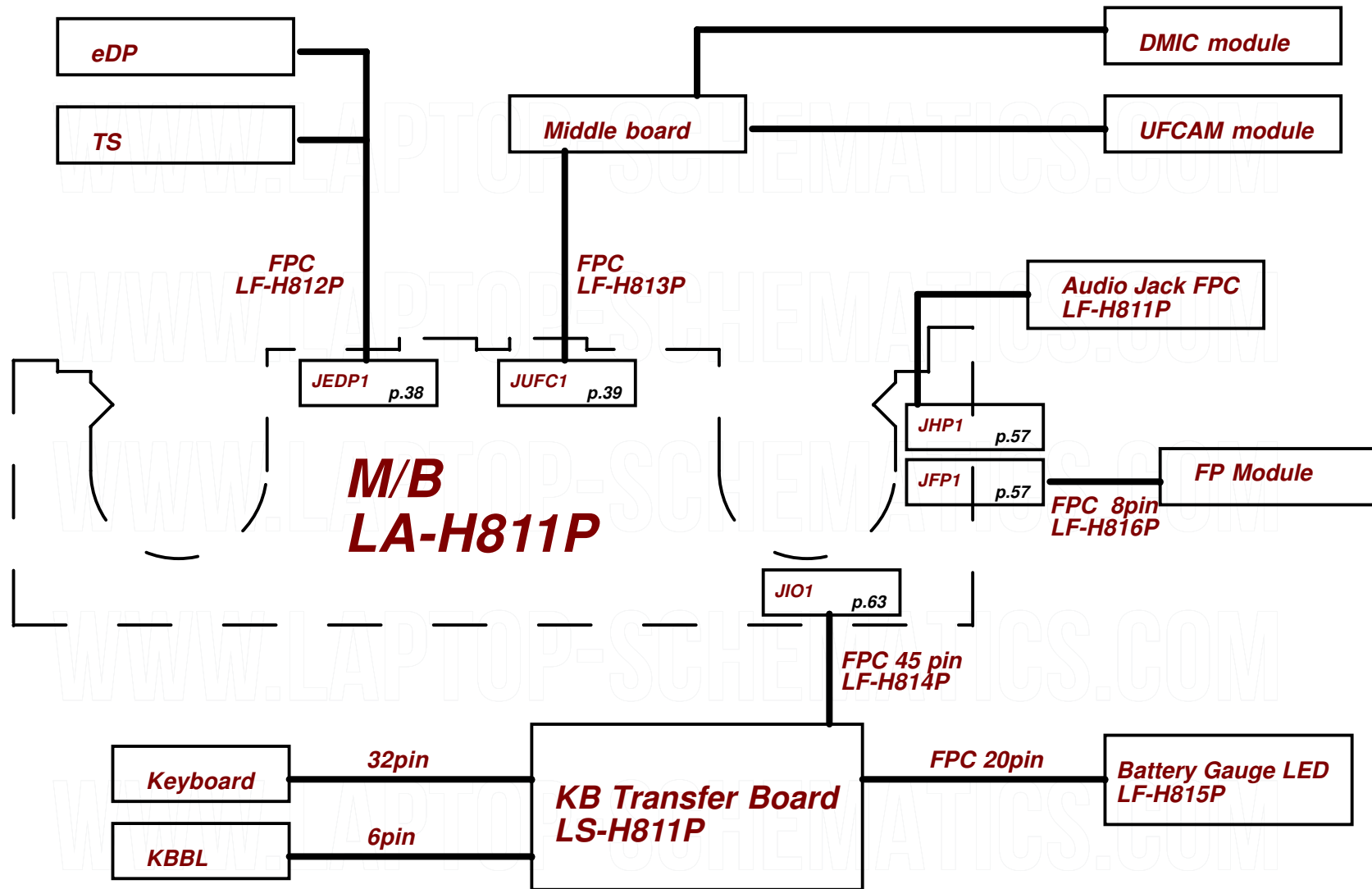
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				Sheet	70 of 100

WLAN



1.8VS





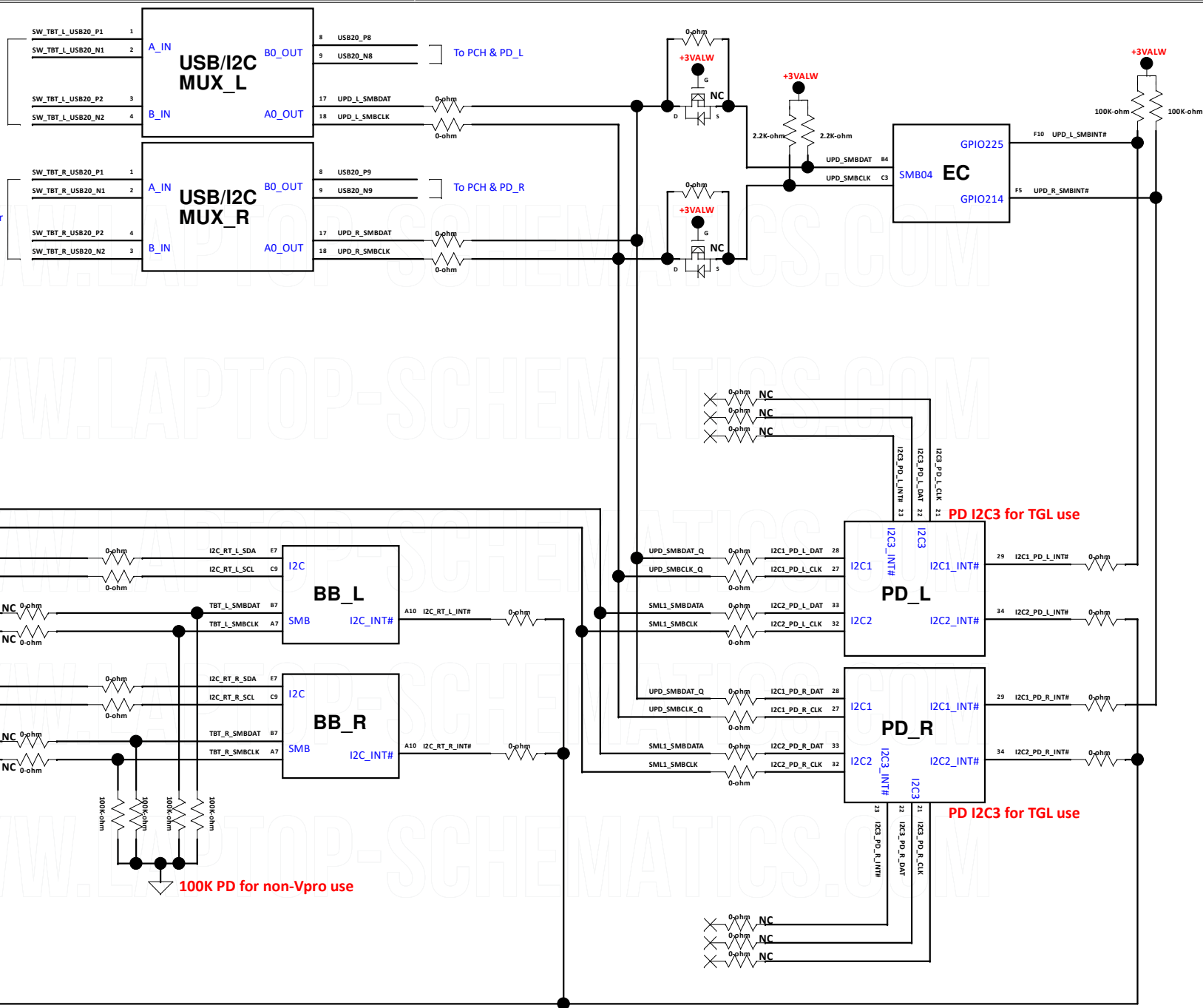
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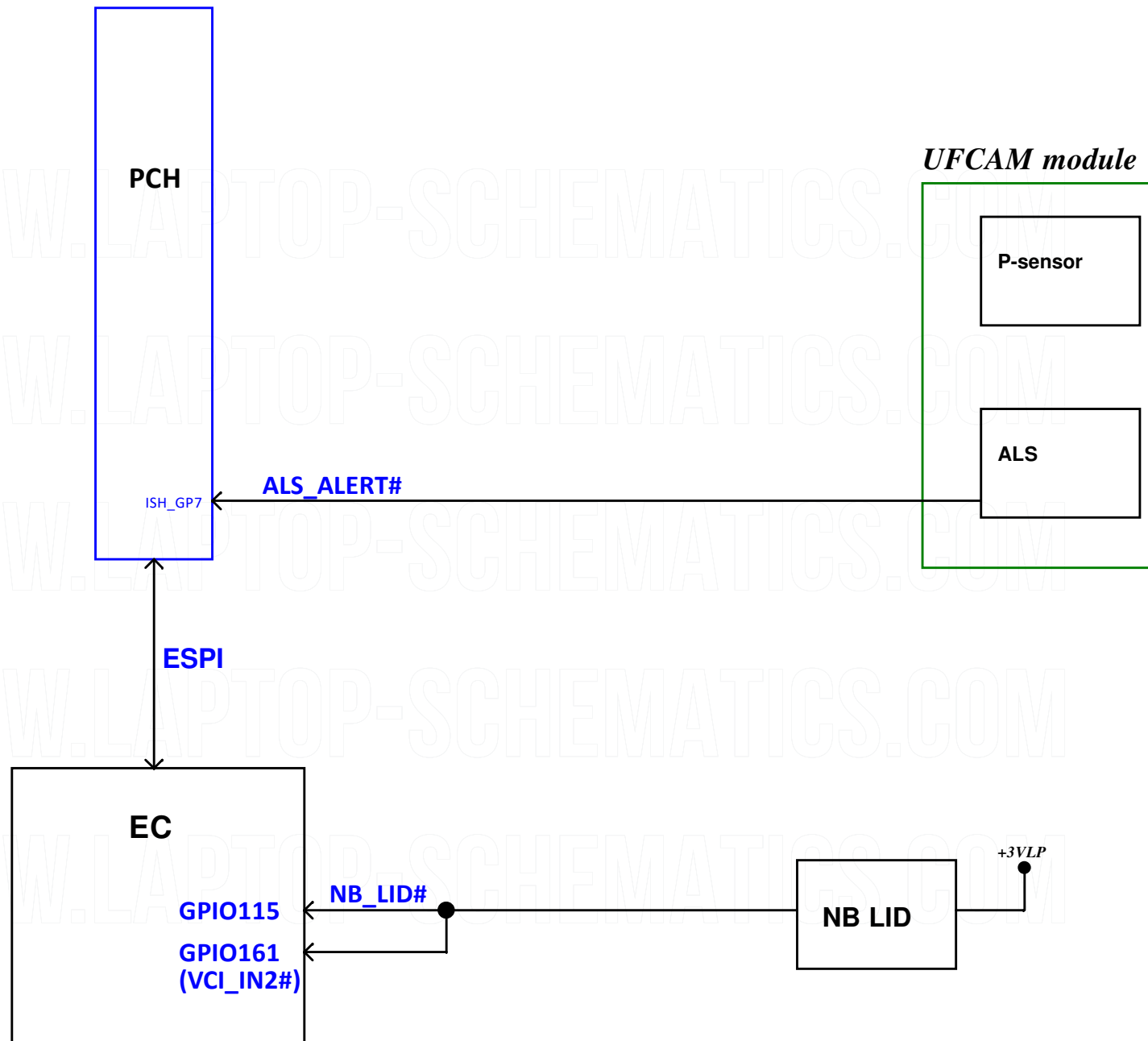
To LEFT Type-C Connector

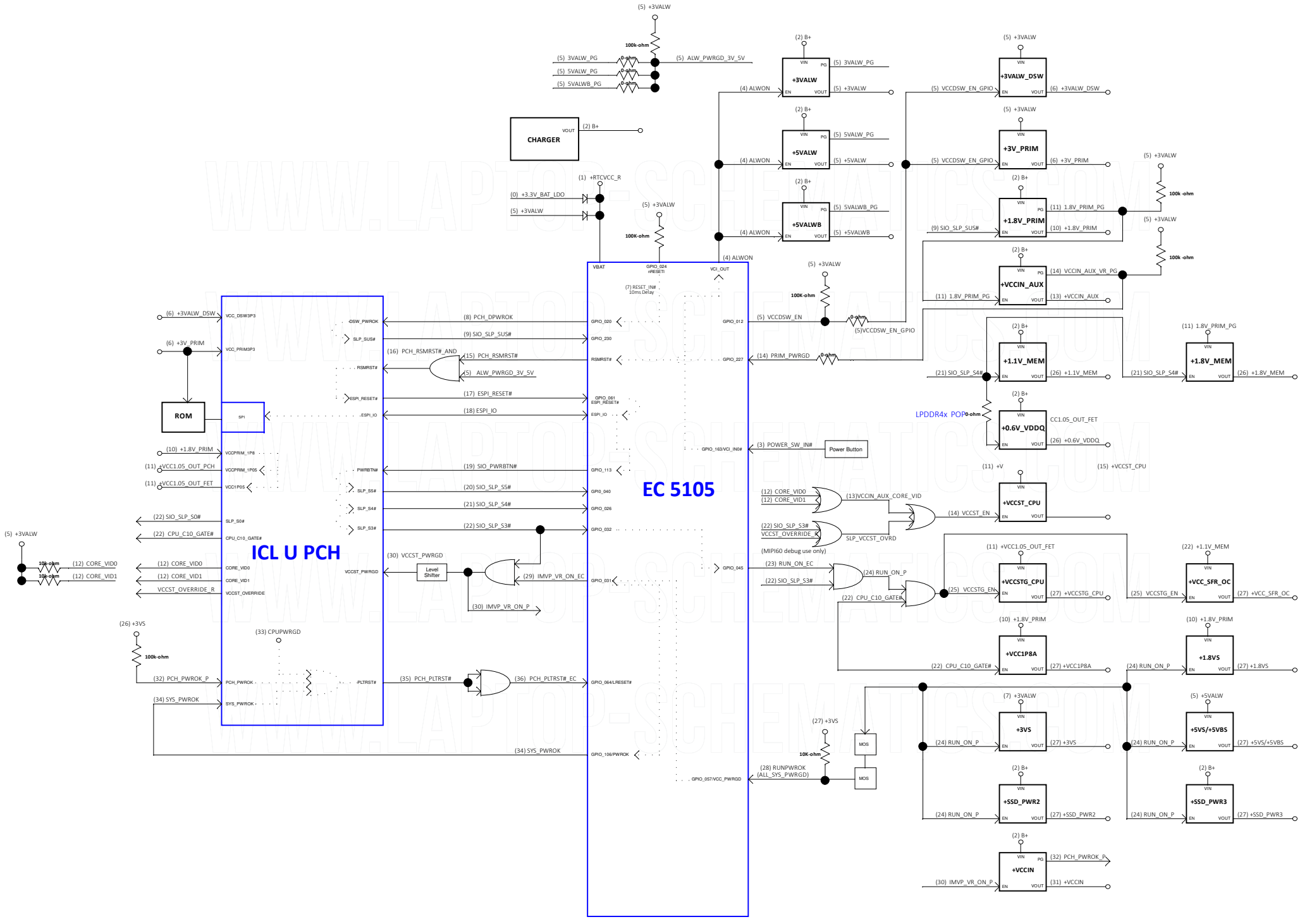
To RIGHT Type-C Connector

PCH

GPP_B11

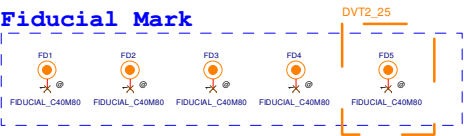




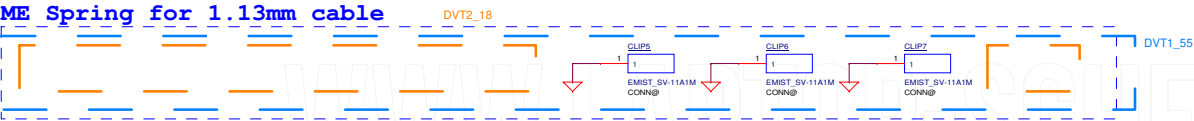


Screw Hole

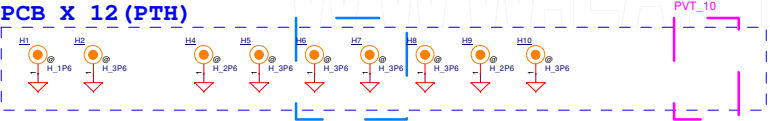
Fiducial Mark



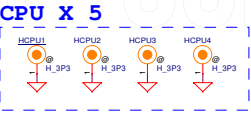
ME Spring for 1.13mm cable



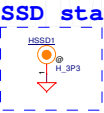
PCB X 12 (PTH)



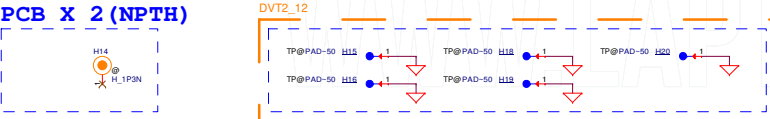
CPU X 5



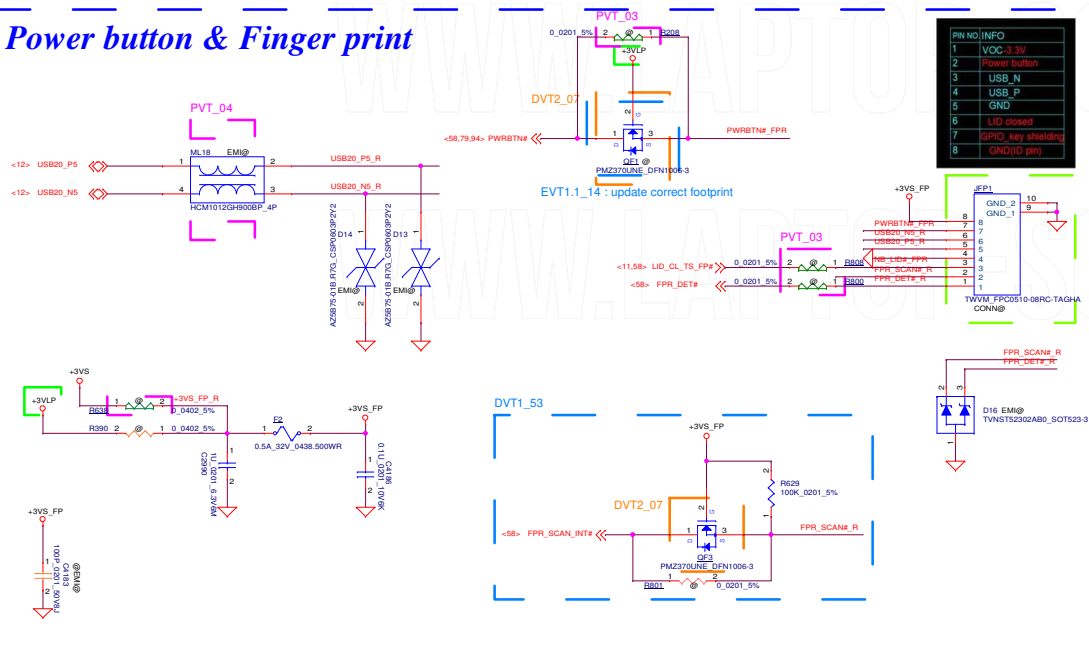
SSD stand-off



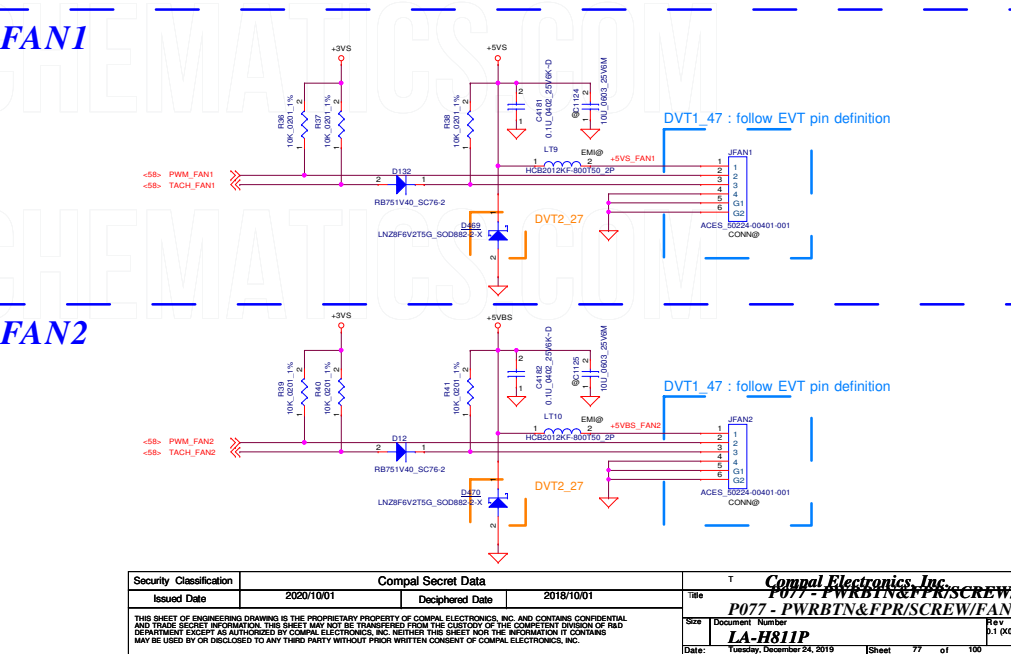
PCB X 2 (NPTH)



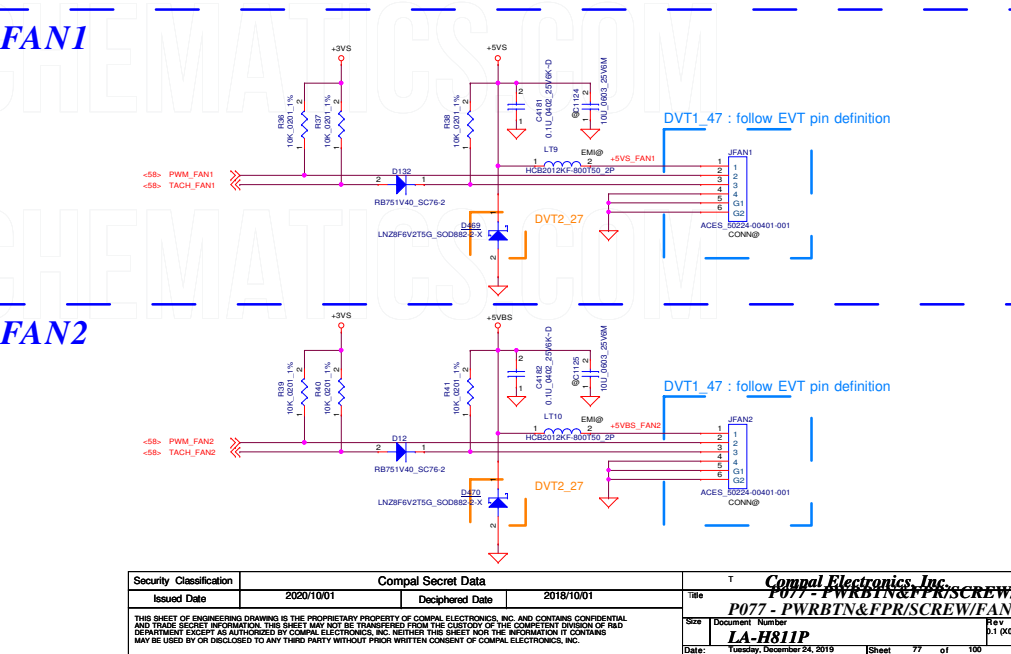
Power button & Finger print



FAN1

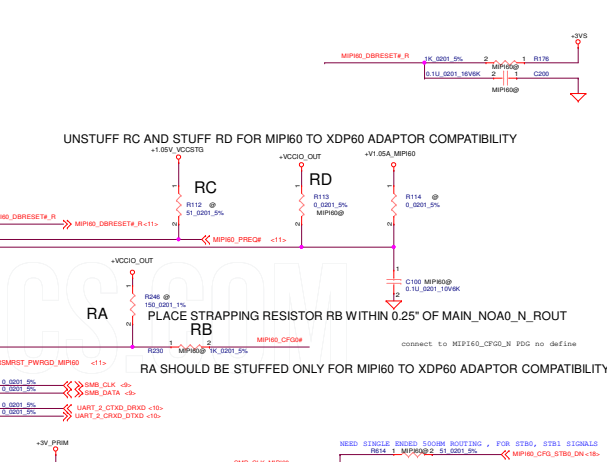
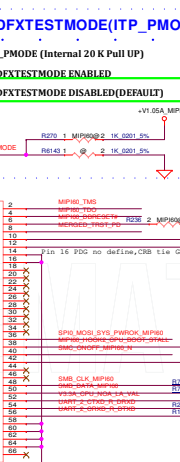
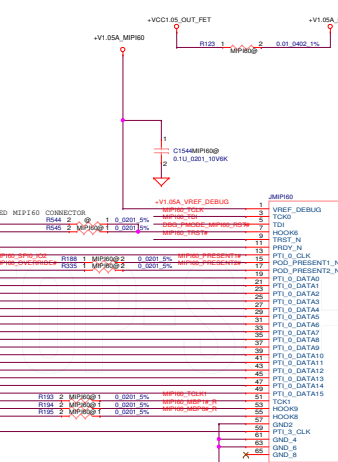
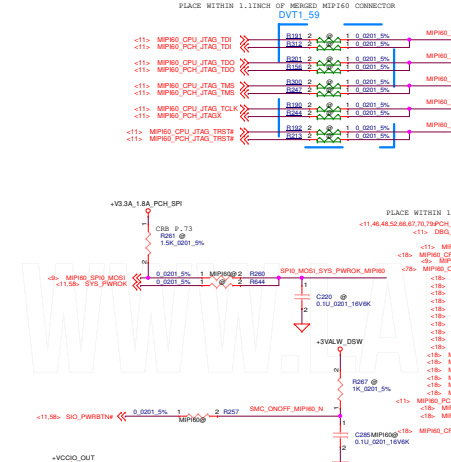
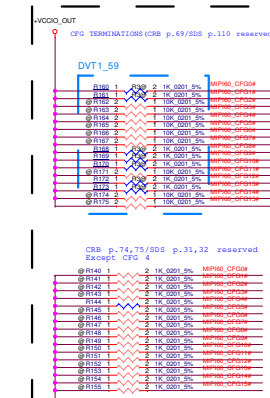


FAN2

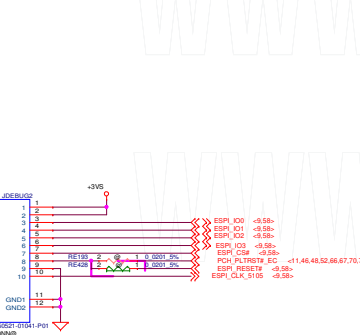
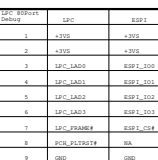


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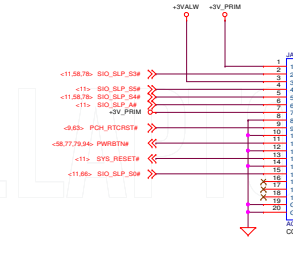
MIP I 60



TFSDT



AP



BIOS UART Debug



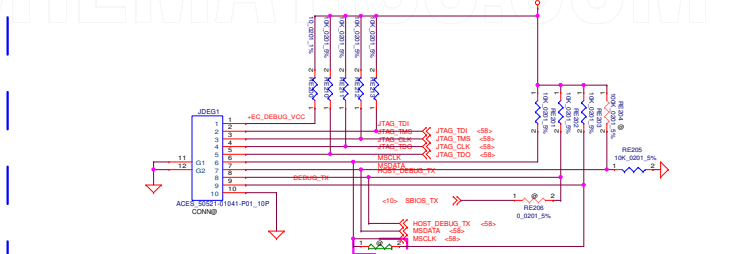
Power Button Debug



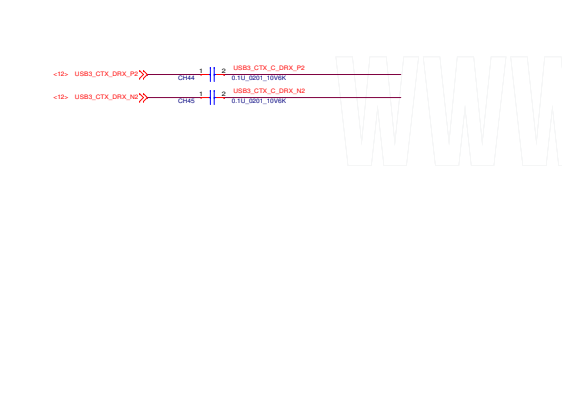
Debuq LED



```
JDEG1
EC UART Debug/80 port
```



DCT Dobu



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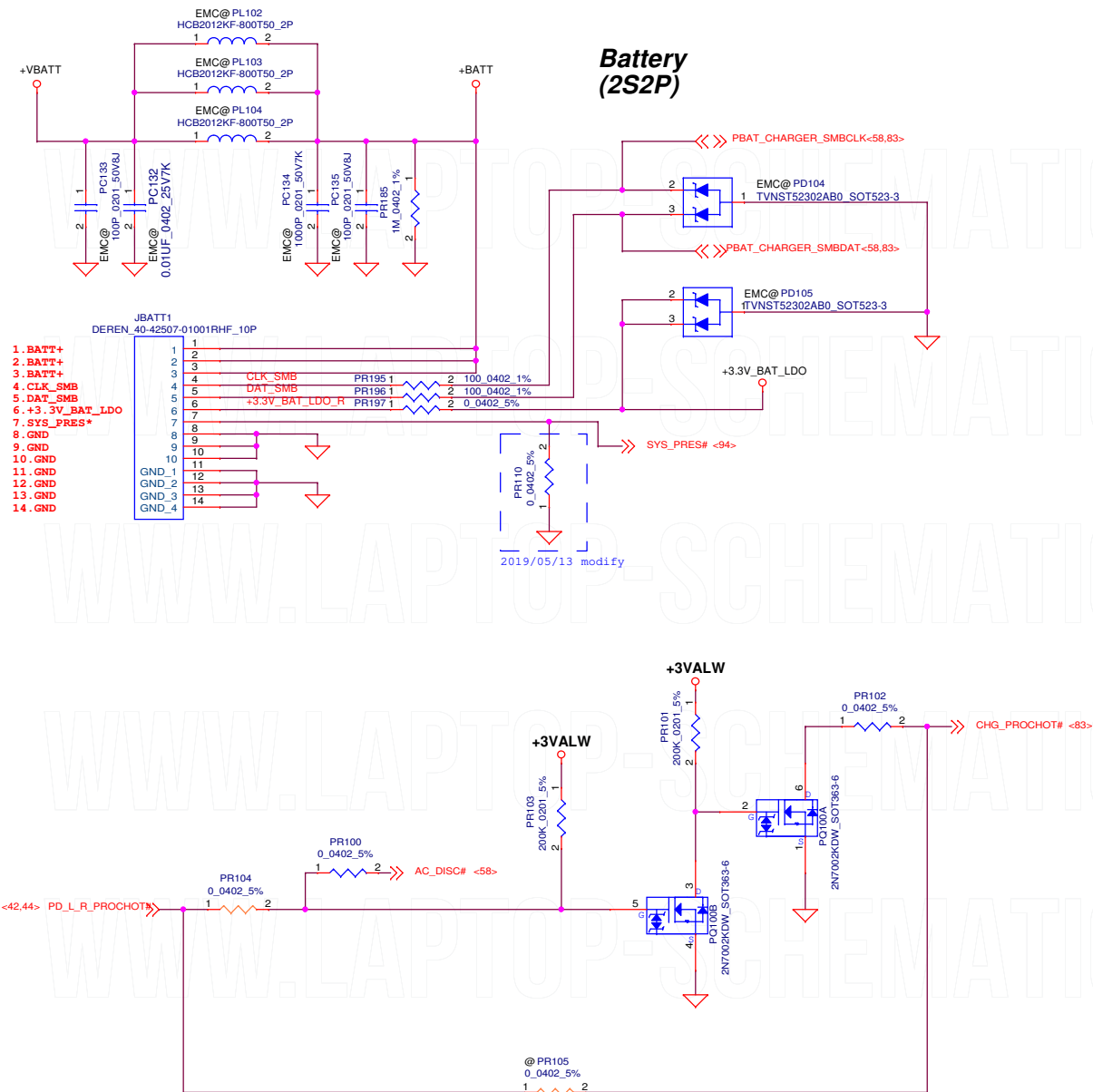
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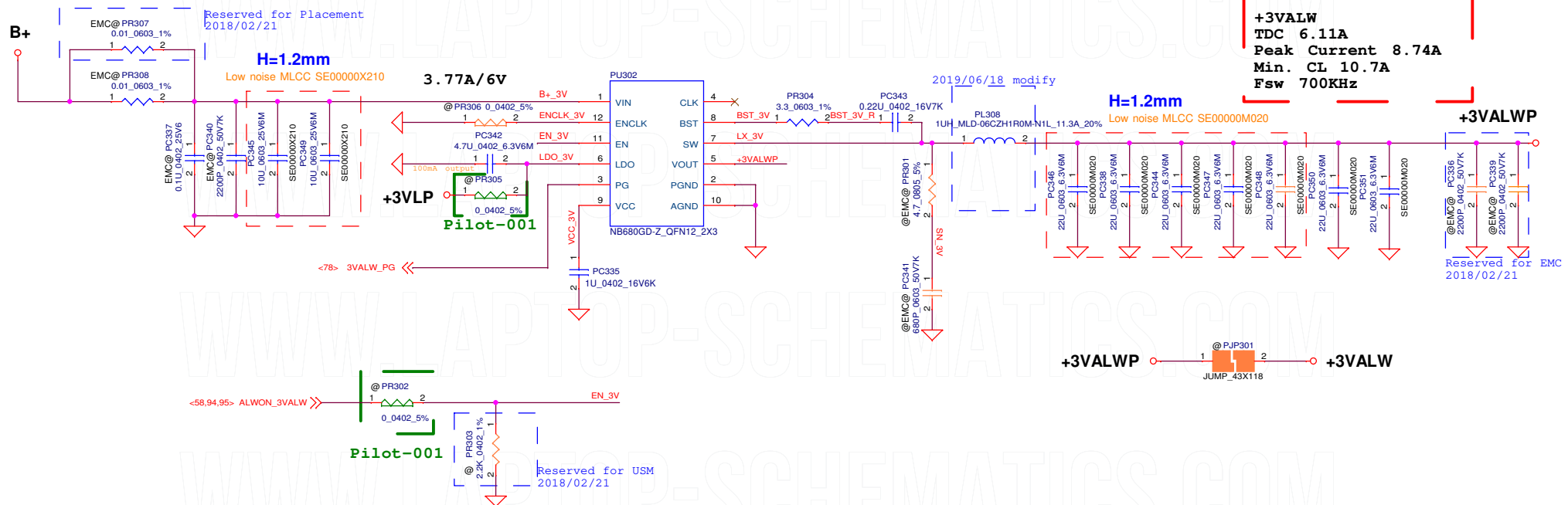
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				PWR POWER BLOCK DIAGRAM		
				Size Document Number		
				LA-G172P		Rev
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				Sheet 81 of 100		

DCIN(37.1)



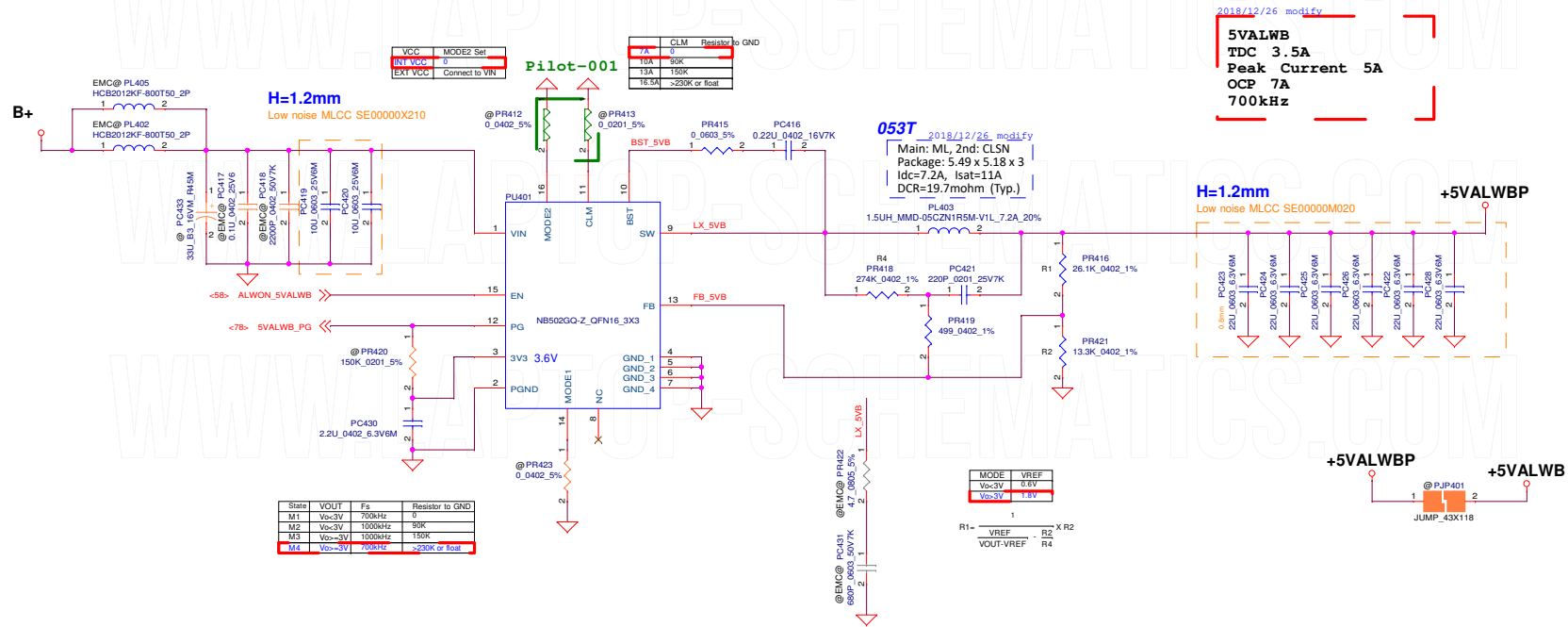
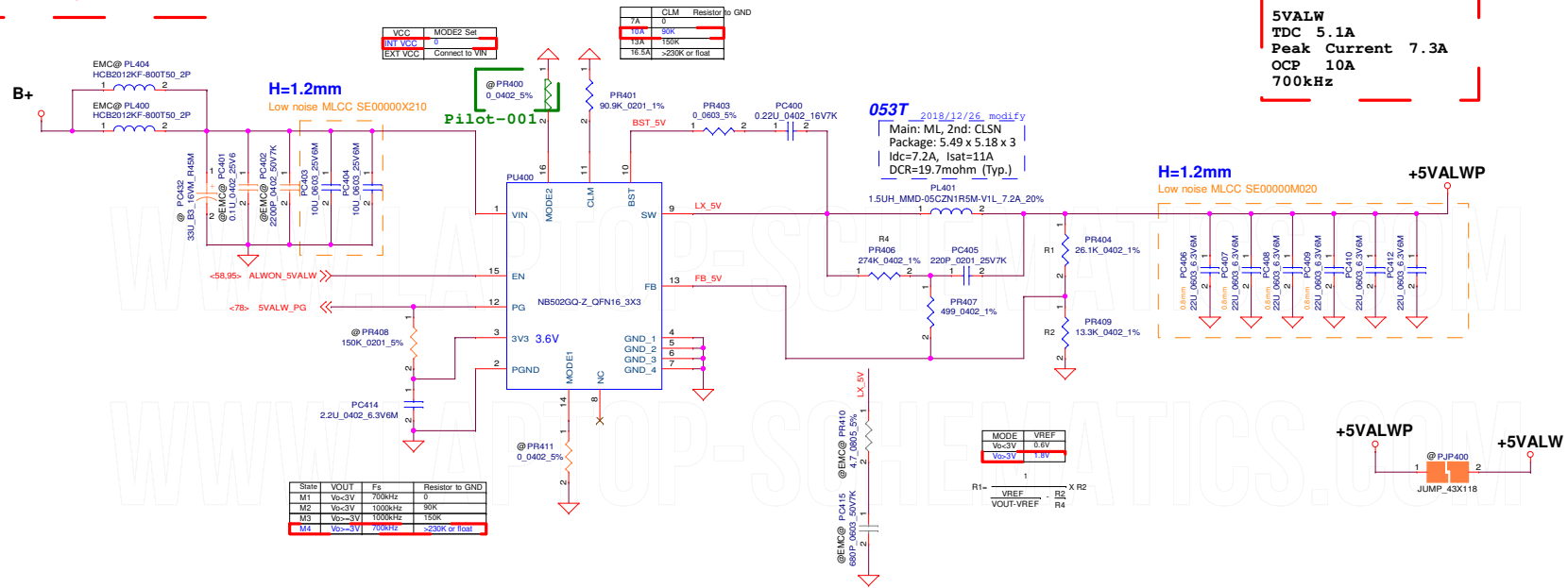
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Controller(35.1), Support component(35.2)



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Controller(35.1), Support component(35.2)



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Controller(35.3), Support component(35.4)

2018/12/26 modify

```
+1.1V_MEM
TDC 4.2A
Peak Current 6A
Min. CL 12A
Fsw 700KHz
```

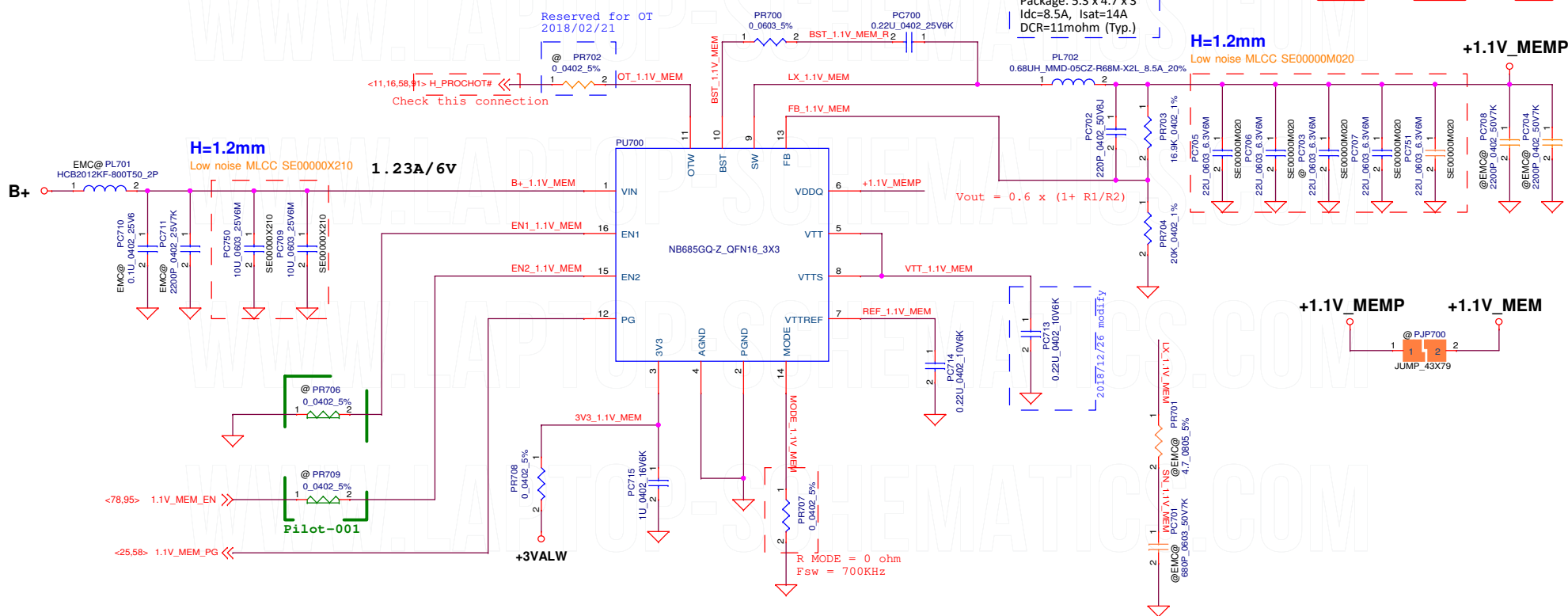
053T

2018/12/26 modify
in: ML, 2nd: CLSN
package: 5.3 x 4.7 x 3
=8.5A, Isat=14A
R=11mohm (Typ.)

$H=1.2\text{mm}$

Low noise MLCC SE00000M020

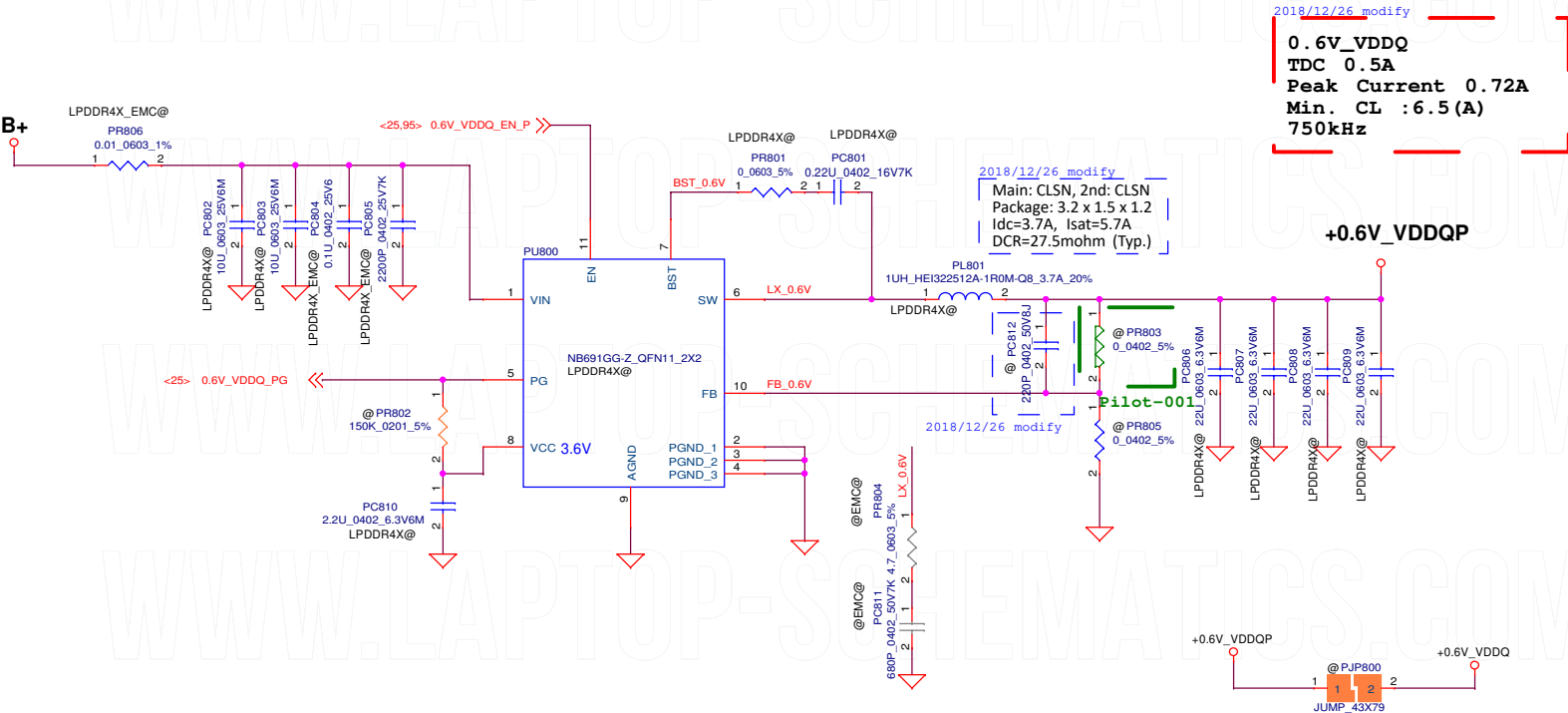
+1.1V MEMP



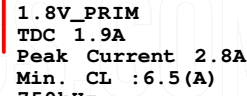
Mode	EN1	EN2	VDDQ	VTT
S0	H	H	on	on
S3	L	H	on	off
S4/S5	L	L	off	off

Note: S3 - sleep ; S5 - power off

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Controller(36.1), Support component(36.3)

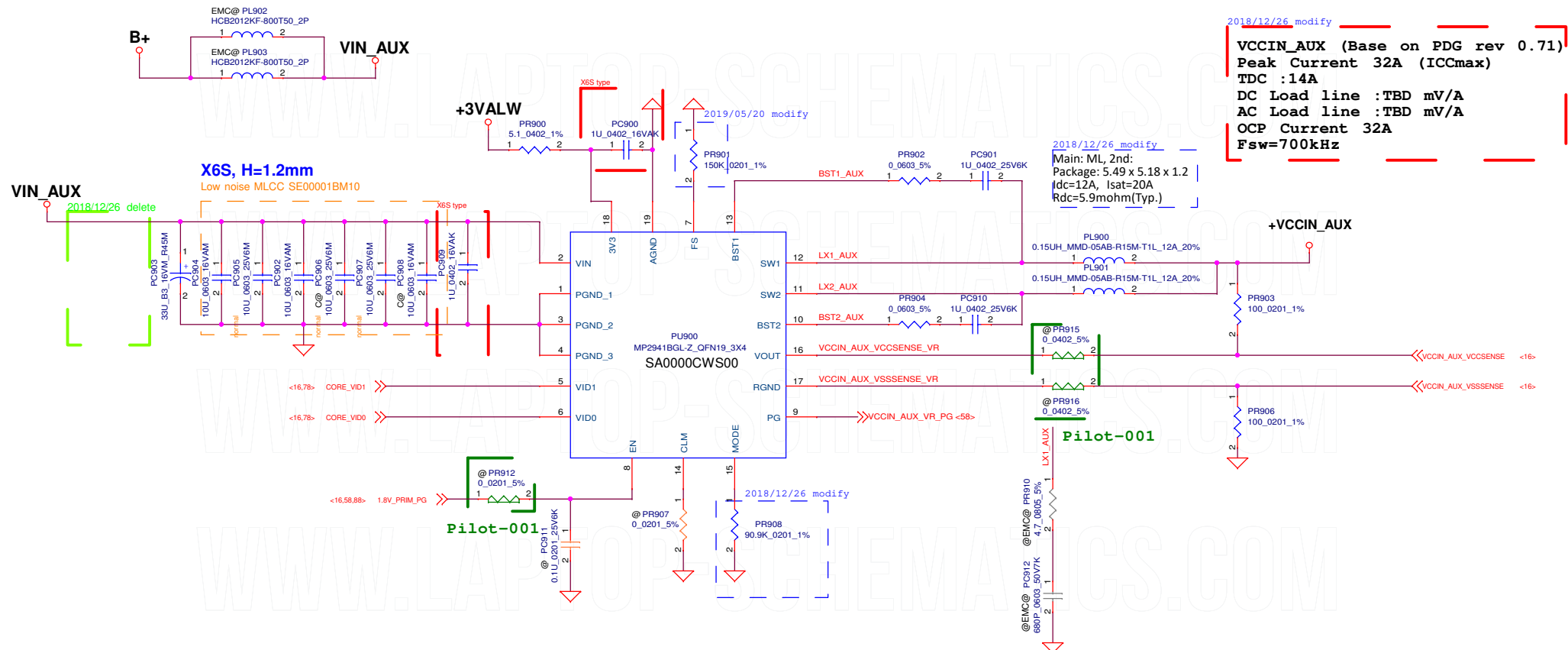


Table---1:VID control Bit logics

VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

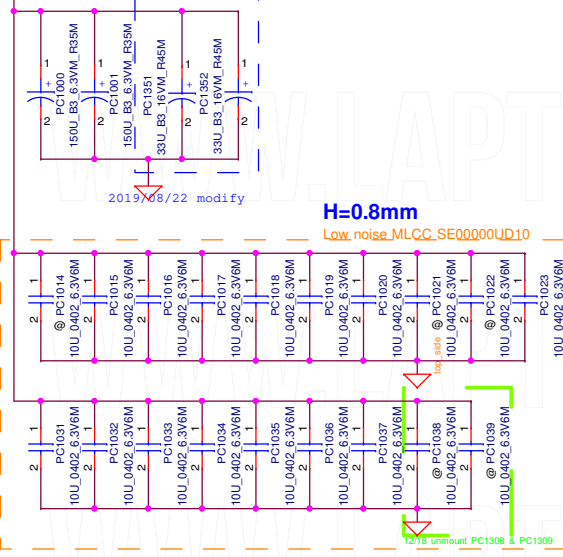
State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs (kHz)	Resistor to GN
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

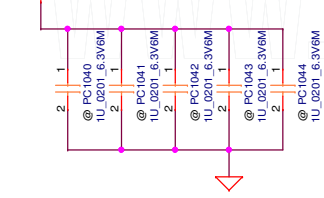
Primary side

+VCCIN_AUX

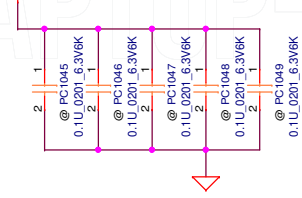


Backside

+VCCIN_AUX



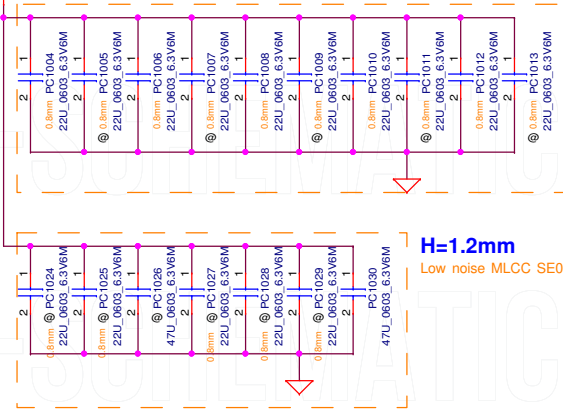
+VCCIN_AUX



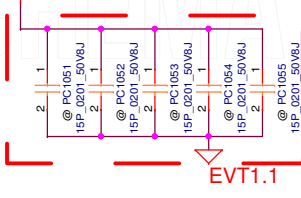
+VCCIN_AUX

H=1.2mm

Low noise MLCC SE00000M020



+VCCIN_AUX

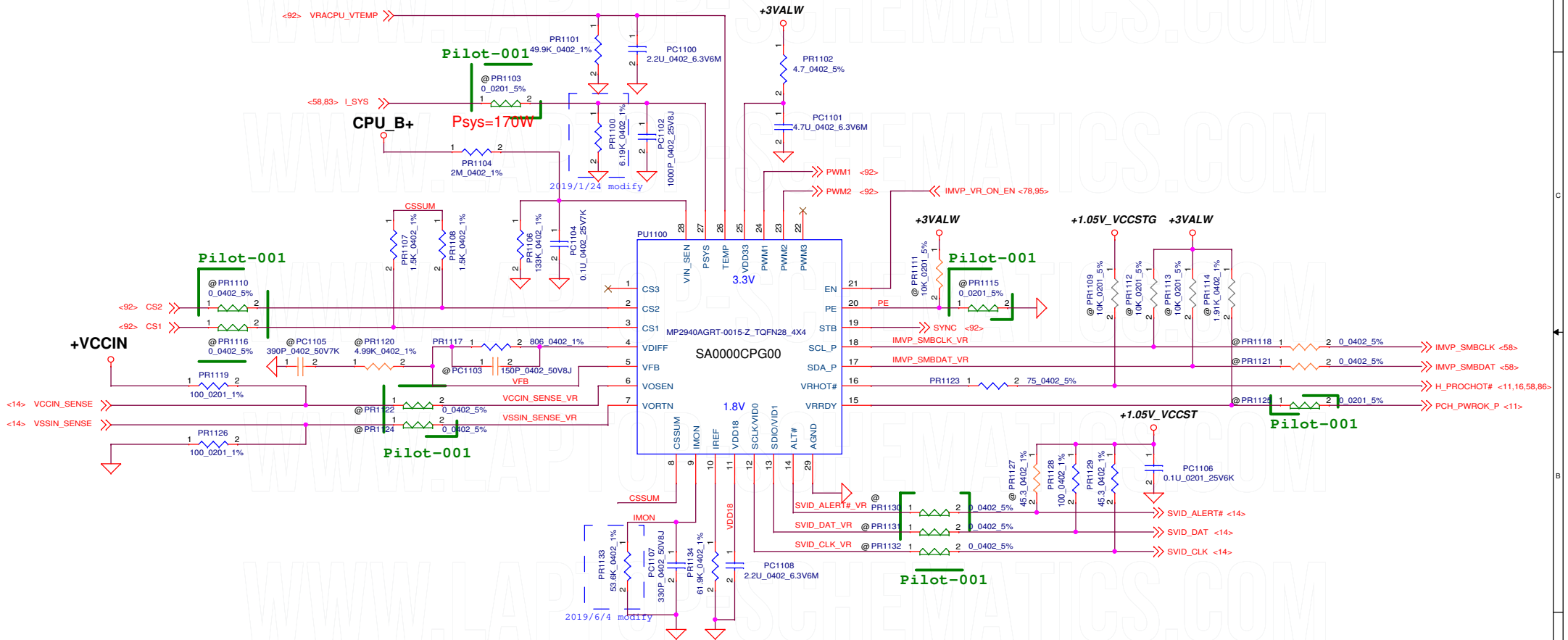


150U_B3 * 4 (POP*2, NC*2)
10U_0402 * 19 (POP*14, NC*5)
22U_0603 * 10 (POP*1, NC*9)
47U_0603 * 7 (POP*1, NC*6)
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)

PDG ver 1.1 Primary side:
2x 330uF 7343
3x 22uF 0603
12x 10uF 0402
1x 47uF 0805

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VCCIN (Base on PDG rev 0.71)
Peak Current 54A (ICCmax)
TDC :25A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz

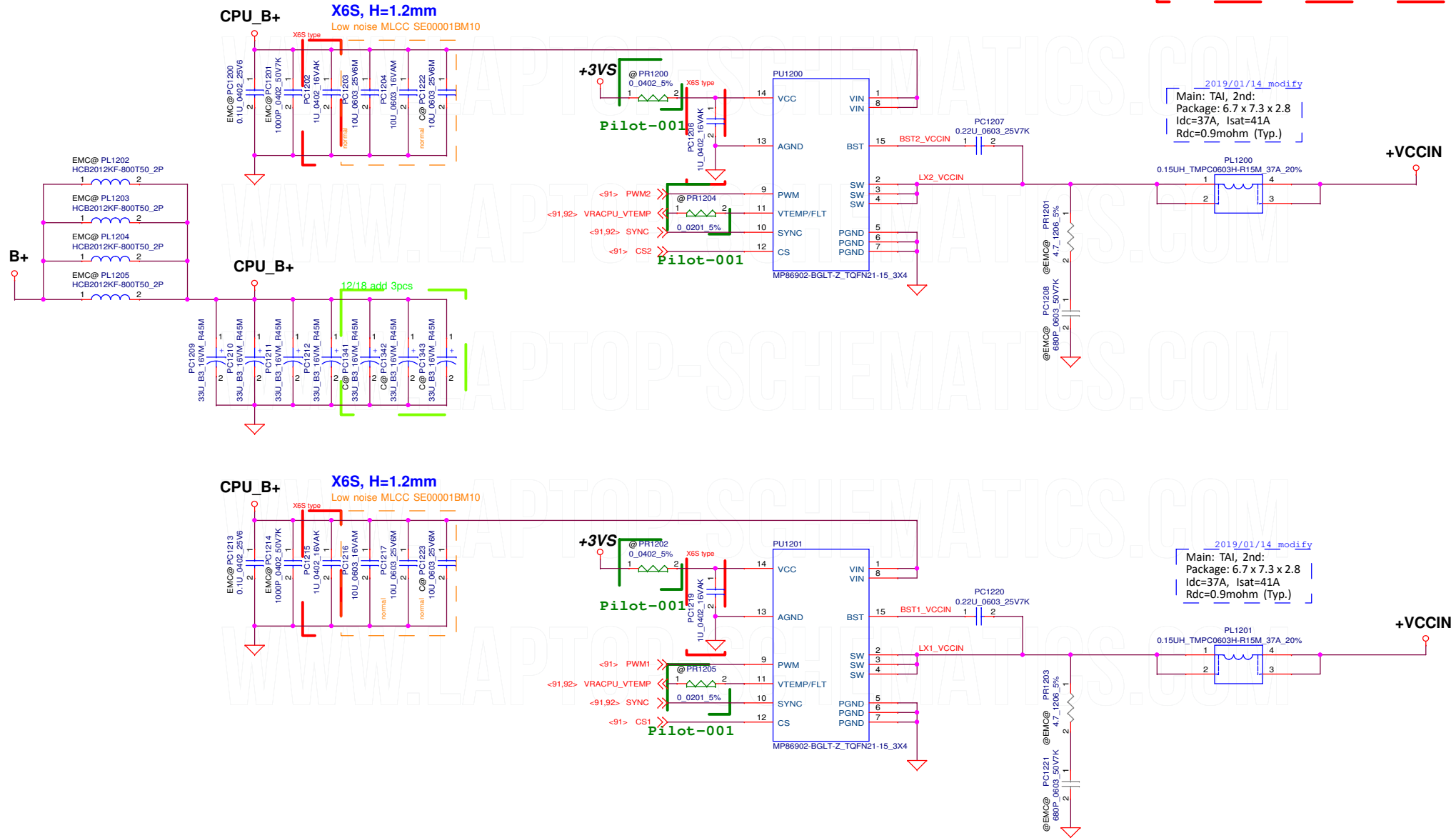


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Support component(36.2),(36.3)

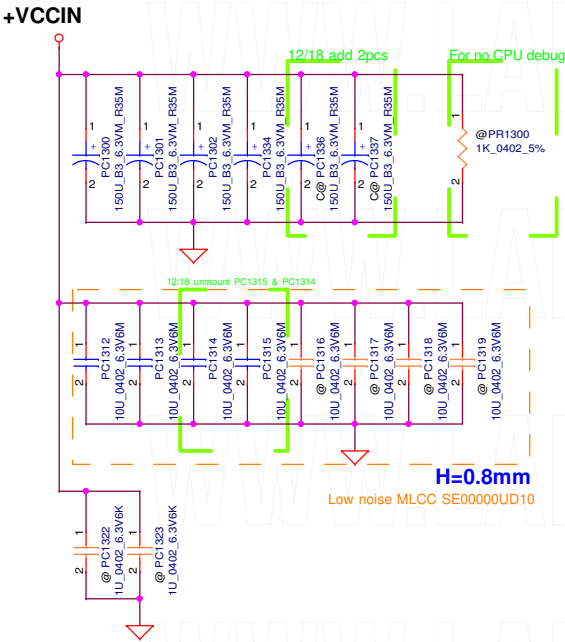
2018/12/26 modify

VCCIN (Base on PDG rev 0.71)
Peak Current 62A (ICCmax)
PL2 TDC :36A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz



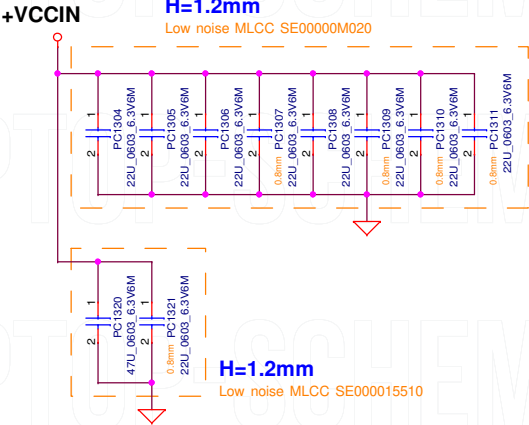
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Primary side

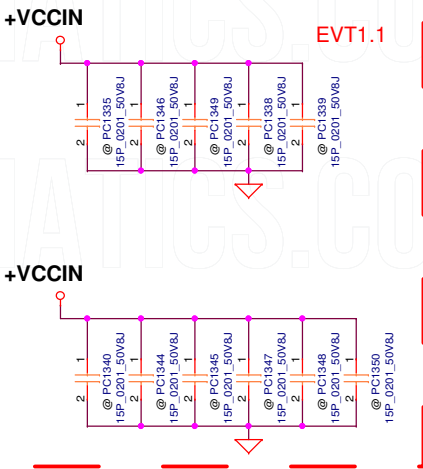
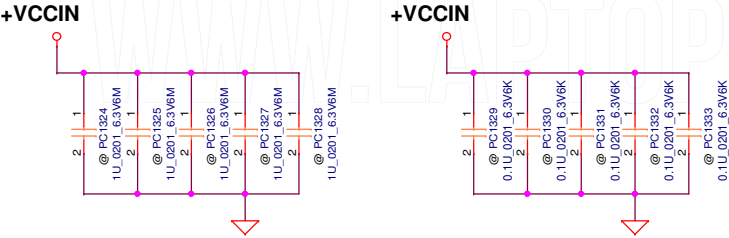


150U_B3 * 4 (pop*2, NC*2)
10U_0402 * 8 (pop*4, NC*4)
22U_0603 * 8 (pop*7, NC*1)
47U_0603 * 2 (NC*2)
1U0402 * 2
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)

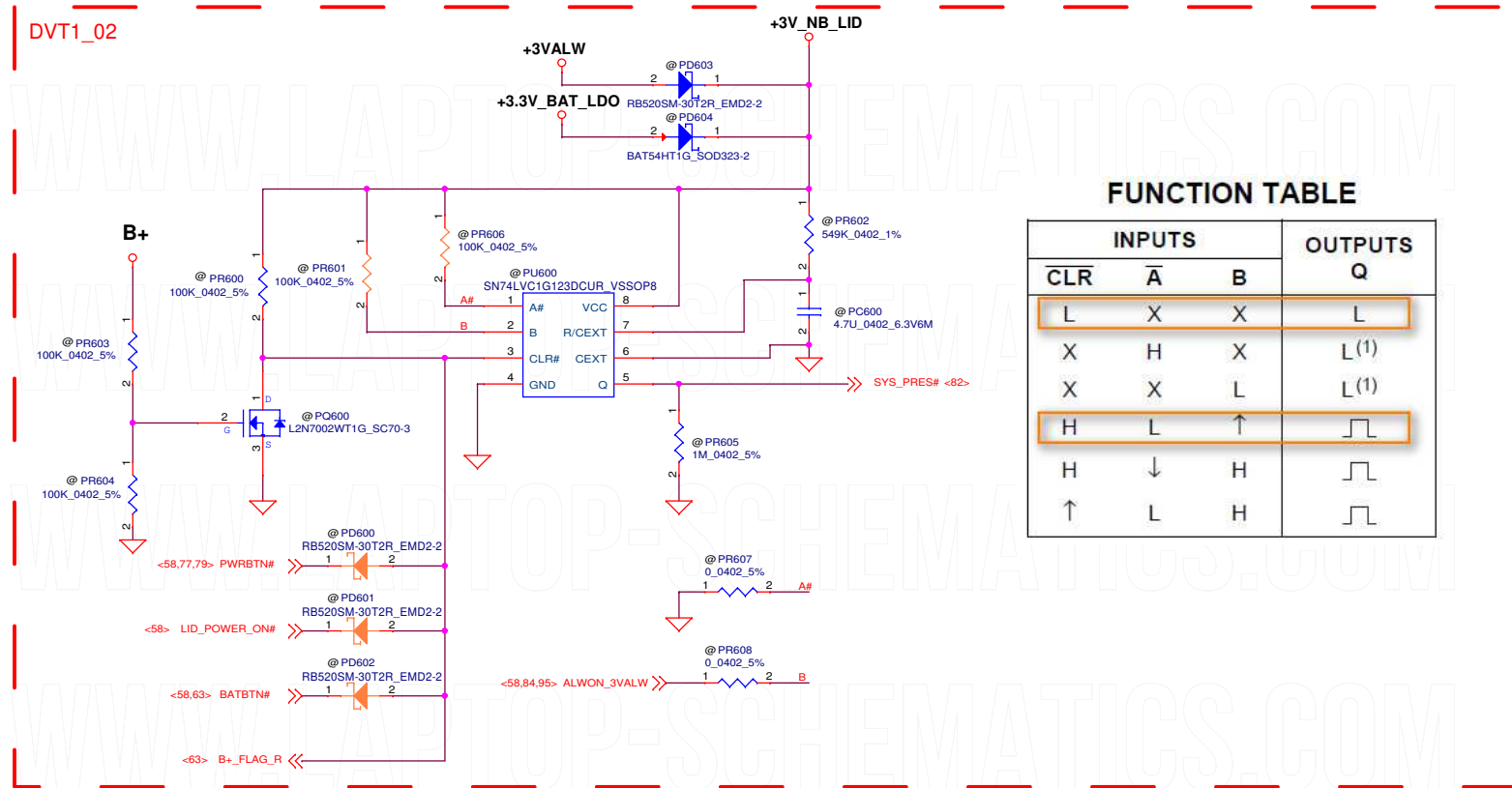
PDG ver 1.1 Primary side:
2x 1uF 0402
4x 10uF 0402
8x 22uF 0603
1x 47uF 0805
2x 330uF 7343

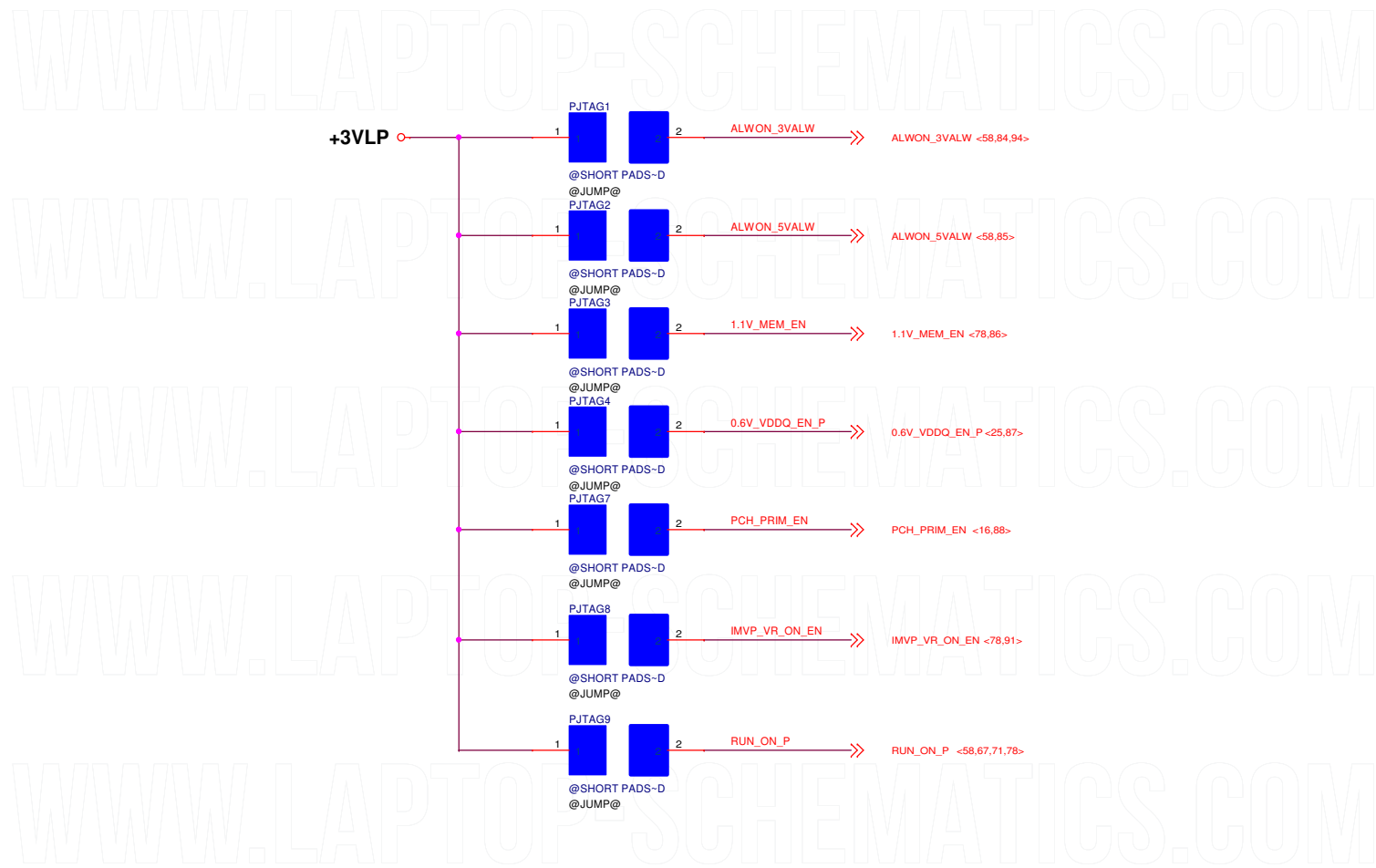


Backside



Support component(37.1)





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